February 2012
Revision 1.1

NPCA110D Audio Enhancing Engine

General Description

The Nuvoton NPCA110D device is a member of Nuvoton's Sound Enhancing family optimized for Audio applications that use a digital (I2S) interface.

The NPCA110D integrates Waves® MaxxAudio 3 sound enhancement algorithms. These are proprietary, patented, psychoacoustic algorithms that compensate for the acoustic limitations of small CE devices.

The MaxxAudio 3 algorithms enable reproduction of rich content, with a wide dynamic range and a full frequency range, on a limited audio system. For low-frequency reproduction, MaxxBass® uses a patented psychoacoustic technique to create a perceived low bass, which can be extended up to 1.5 octaves lower than the original. This technique reproduces full and rich sounding bass tones. Power handling is done by MaxxVolume, which utilizes the power amplifiers and speakers to their full extent yet avoids clipping and distortions.

The MaxxAudio 3 software suite provides additional algorithms that enhance the overall sound quality, such as Maxx3D, which widens the stereo image, and MaxxTreble for reproducing crystal clear high frequencies. To design a resonance-free audio system, MaxxEQ provides a flexible equalizer with 10 bands.

Specifically designed for devices such as TV, MaxxLeveler maintains a constant level of output for any given content. This feature is useful for maintaining the same volume during commercials or when switching TV channels.

The Maxx family of devices includes:

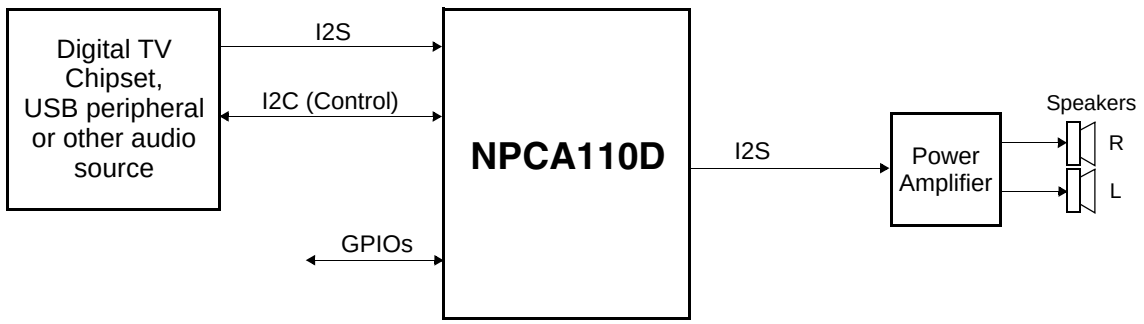
- High-performance, 24-bit audio enhancing engine pre-programmed with Waves MaxxAudio 3 algorithms
- Optional audio DAC
- Optional audio ADC
- Digital I/O and other features for high-performance audio systems

The MaxxAudio Graphical User Interface (GUI) enables sound engineers to easily tune the device and customize presettings for different audio products.

Outstanding Features

- Improves audio quality for low-performance speakers
- System-level BOM savings
- Stereo operation
- I2C controlled
- 24-bit accuracy
- Audio algorithms
  - MAXXBASS®
  - MAXX3D
  - MAXXTREBLE
  - MAXXEQ
  - MAXXVOLUME®
  - MAXXLEVELER
  - MAXXDIALOG
- Audio input
  - Up to three I2S or Synchronous Serial Interface (SSI) inputs
- Audio output
  - Optional generation of one bass channel
  - Up to three I2S or SSI outputs
- Several General-Purpose digital signals available to the application (GPIOs)
- Typical operational power target of less than 0.2W
- Power-down target of less than 3 mW
- 3.3V operation

System Block Diagram



Features

Bus Interfaces

- Synchronous Serial Interface (SSI)
  - Compatible with I2S
  - Master and slave timing support
- I2C Interface
  - Compliant with *I2C-BUS Specification Revision 1.0, 1992*
  - Master or slave interface
  - Supports 7-bit address mode

Audio Enhancing Engine

- Processing Unit
  - 24-bit accuracy
  - 125 MIPs

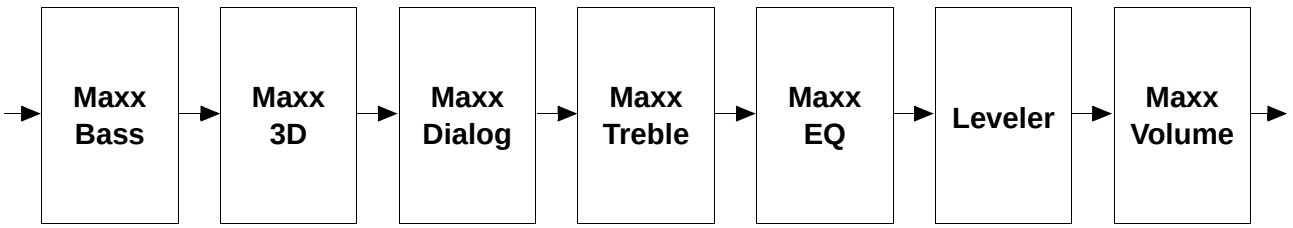
Audio Algorithms

- Sample frequency of 44.1 KHz or 48 KHz supported
- MaxxBass®
  - Patented Waves MaxxBass psycho-acoustic bass extension delivers a more natural sound than traditional bass boost technologies, which use EQ and can overpower your system. MaxxBass analyzes low frequencies to create harmonics that are perceived as lower, deeper tones.
- Maxx3D
  - Maxx3D extends the span of stereo-side content while maintaining the integrity of unprocessed center content.
  - Maxx3D for Speakers improves the stereo separation of speakers, widening the stereo field for optimal imaging.
  - Maxx3D for Headphones improves stereo perception, restoring the original listening balance to provide more natural sound.
- MaxxTreble
  - MaxxTreble delivers crystal clear high-frequency enhancement for increased RMS without exceeding the system ceiling. Its proprietary algorithm restores luster to over-compressed formats to provide the perfect listening experience.
- MaxxEQ
  - MaxxEQ provides the ability to design EQ curves and shape sound with surgical precision, using up to 10 programmable filters with bell, shelf, low pass, and high pass, plus adjustable frequency, gain, and Q parameters. MaxxEQ's intuitive Graphic User Interface makes click-and-drag filter design fast and easy.
- MaxxVolume®
  - MaxxVolume is an all-in-one volume control, with High-Level Compression to increase RMS levels, Low-Level Compression to increase the clarity of soft sounds, Noise Gating to eliminate signal and system noise, and Leveling to smooth out volume levels.
- MaxxLeveler
  - MaxxLeveler regulates the perceived volume of the audio, keeping all audio content at the same level.
- MaxxDialog
  - MaxxDialog is a revolutionary new technology that enables users to adjust center channel dialog levels without affecting the rest of the audio mix. Based on the Waves Center pro audio plug-in, MaxxDialog delivers clear, crisp dialog that does not disappear behind loud music and effects.
- Sub-Woofer
  - Enables separating low-frequency content and directing it into a third audio channel, for driving a subwoofer.

Straps, Clocks, Supply and Package Information

- Strap Input Controlled Operating Modes
  - PLL reference clock select (REF strap)
  - Test mode select (nTEST strap)
  - I2C master or slave select (I2CMS strap)
  - Boot options
    - ROM code operation
    - Loadable algorithms for new functions or ROM code patching
- Input Clocks
  - SSI / I2S clock: 64 x sample frequency
  - Optional crystal oscillator or input clock
- Power Supply
  - 3.3V supply operation
- Power-Save Modes
  - Clock switch to a lower frequency
  - WAIT instruction (clock stopped)
  - PLL power-down
- Package
  - 5 x 5 mm, 32-pin Quad Flat No-Lead (QFN)

Algorithm Processing Chain



Features (Continued)

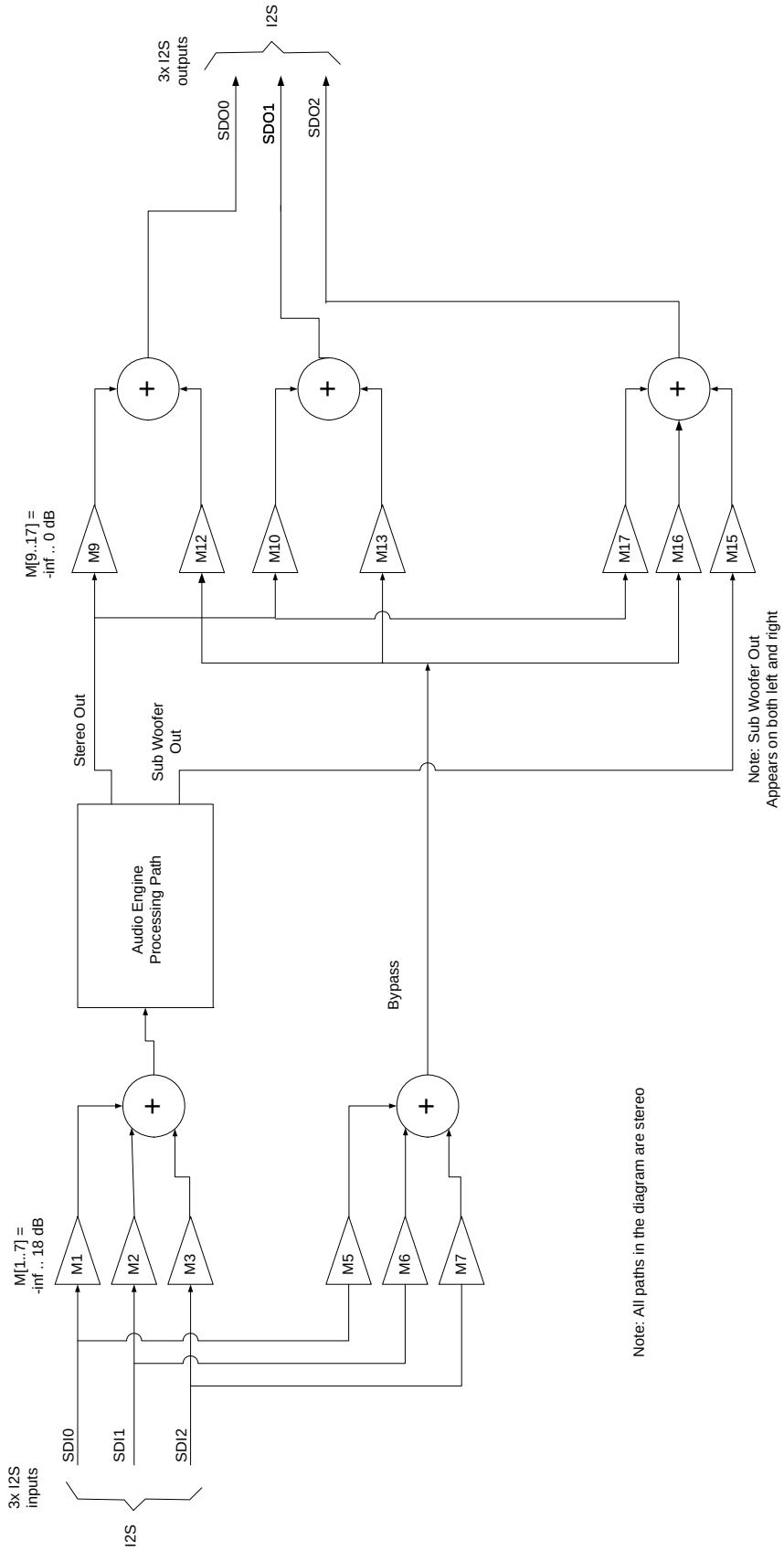


Figure 1. Device Block Diagram

Revision Record

Date	Status	Comments
June 2011	Revision 0.75	Datasheet first revision.
June 2011	Revision 0.75	Changes: • Added algorithm processing Chain diagram • Added block diagram • Added Clocks section in Chapter 2 • Added current consumption in Electrical Specification • Various small changes
August 2011	Revision 0.80	Changes: • Pins: Corrected that SDA and SCL are OD6 pins • Power and Reset: — Removed TBD from crystal circuit — Added Clocks section • Electrical Specifications: — Changed input type ST V_{IH} level to minimum 2.0 V, V_H to 280 mV — Section 4.2.5: Changed maximum leakage of all pins from <30 μA to <10 μA — Changed pull-up resistor minimum value to 34 KΩ — Added that CLKOUT duty cycle is characterized only — Changed I2C timing AC levels to 0.8 and 2.0V — I2C Slave: removed $t_{HD:DS}$ from spec; changed $t_{HD:DAT}$ minimum to 18 ns — SSI slave: Changed t_{HR} minimum to 2 ns
November 2011	Revision 1.0	Changes: • Changed device description • Changed package marking
February 2011	Revision 1.1	Changes: • Fixed typo: “I2CMS” signal is “I2C Master/Slave Strap” (not I2S).

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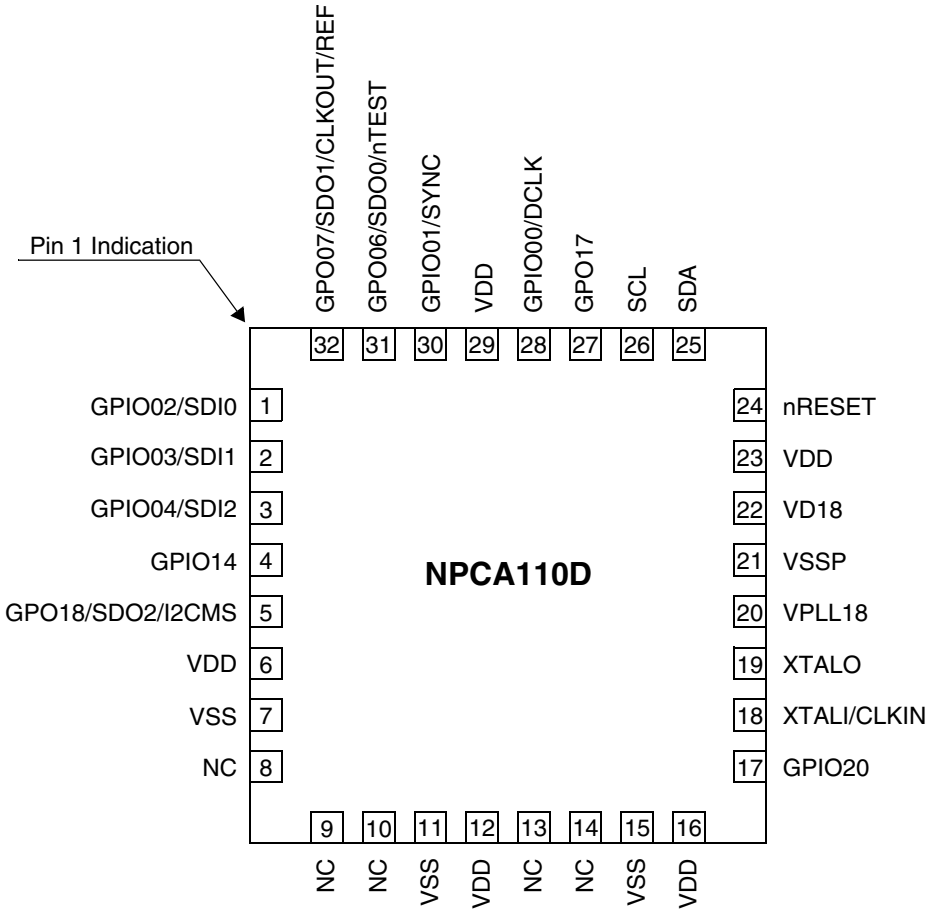
1.0 Signal/Pin Description

1.1 CONNECTION DIAGRAM



Note: Bottom pad is VSS.

32-Pin Quad Flat No-Lead (QFN) Package
Order Number: NPCA110DA0YX

1.0 Signal/Pin Description (Continued)

1.2 PIN TYPES

Table 2. Abbreviations

Abbreviations	Description
GPIO	General-Purpose I/O
GPO	General-Purpose Output
Ox/y	Output, Source x mA, Sink y mA
ODy	Output, Open-Drain, Sink y mA
5V	Input tolerant to 5 volts
PU	Input buffer with a pull-up resistor. This pull-up resistor is intended to maintain unconnected input pins at high logic level. The voltage measured externally on an unconnected input pin is in the range of 1.5 to 2.5V, although the input itself is near V_{DD} level.
T	Input buffer with CMOS / LVTTL levels
ST	Schmitt trigger input buffer with CMOS / LVTTL levels
A	Analog input or output
XO	Crystal Oscillator

1.3 PIN DESCRIPTION

1.3.1 Clocks and Reset

Note: Crystal oscillator connections are found in Figure 3 on page 13.

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
XTALI/CLKIN	I	**Crystal Clock Input**. Used for a crystal connection circuit or as a clock input (clock input at LVTTL levels). The crystal should have a frequency of 12.288 MHz (48 KHz sample rate) or 11.2896 MHz (44.1 KHz sample rate).		VDD	XO	
XTALO	O	**Crystal Clock Output.** Used for a crystal connection circuit.				
nRESET	I	**Power-Up Reset Input.** If driven low, forces reset.	PU	VDD	5V, ST	

1.3.2 GPIO

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
GPO17	O	**General-Purpose Output Signal 17.**	PU	VDD	T, 5V, O8/8	
GPIO20	I/O	**General-Purpose I/O Signal 20.**	PU	VDD	T, 5V, O2/2	
GPIO14	I/O	**General-Purpose Output Signal 14.**	PU	VDD	T, 5V,O8/8	

1.0 Signal/Pin Description (Continued)

1.3.3 I2S / GPIO / STRAPS

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
GPIO00 / DCLK	I/O I/O	**General-Purpose I/O Signal 00.** / **I2S Clock.** Input for an I2S slave and output for an I2S master. The frequency must be either 32 or 64 times the sample frequency. When used as output, a 33Ω to 100Ω series resistor is required.	PU	VDD	T,5V,O2/2	
GPIO01 / SYNC	I/O I/O	**General-Purpose I/O Signal 01.** / **I2S SYNC.** Input for an I2S slave and output for an I2S master. Indicates the sample frequency. When used as output, a 33Ω to 100Ω series resistor is required.	PU	VDD	T,5V,O2/2	
GPIO02 / SDI0	I/O I	**General-Purpose I/O Signal 02.** / **I2S Serial Data In 0.** Carries input stereo data stream 0.	PU	VDD	T,5V,O2/2	
GPIO03 / SDI1	I/O I	**General-Purpose I/O Signal 03.** / **I2S Serial Data In 1.** Carries input stereo data stream 1.	PU	VDD	T,5V,O2/2	
GPIO04 / SDI2	I/O I	**General-Purpose I/O Signal 04.** / **I2S Serial Data In 2.** Carries input stereo data stream 2.	PU	VDD	T,5V,O2/2	
GPO06 / SDO0 / nTEST	O O I	**General-Purpose Output Signal 06.** / **I2S Serial Data Out 0.** Carries output stereo data stream 0. A 33Ω to 100Ω series resistor is required. / **Test Strap.** Sampled during Power-Up reset. The pin is pulled up by an internal resistor for normal operation or set to 0 by an external 8.2 KΩ pull-down resistor.	PU	VDD	T,5V,O2/2	
GPO07 / SDO1 / CLKOUT / REF	O O O I	**General-Purpose Output Signal 07.** / **I2S Serial Data Out 1.** Carries output stereo data stream 0. / **General-Purpose Clock Output.** A 33Ω to 100Ω series resistor is required. / **Reference Strap.** Sampled during Power-Up. The pin is pulled up by an internal resistor (selects DCLK in) or set to 0 by an external 8.2 KΩ pull-down resistor (selects crystal oscillator).	PU	VDD	T,5V,O2/2	
SDO2 / GPO18 / I2CMS	O O I	**I2S Serial Data Out 2.** Carries output stereo data stream 0. A 33 to 100 Ω series resistor is required. / **General-Purpose Output Signal 18.** / **I2C Master/Slave Strap.** Sampled during Power-Up reset. The pin is pulled up by an internal resistor (selects slave) or set to 0 by an external 8.2 KΩ pull-down resistor (selects master).	PU	VDD	T,5V,O2/2	

1.0 Signal/Pin Description (Continued)

1.3.4 I2C / GPIO

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
SDA	I/O	**Master/Slave I2C Data Line.**		VDD	ST,5V,OD6	
SCL	I/O	**Master/Slave I2C Clock Line.** When used as an input, ignores short pulses of a length of less than 5 ns and rejects more signal changes within 20 ns (reducing signal reflections hazards).		VDD	ST,5V,OD6	

1.3.5 Power

Note: Power connections are found in Figure 1 on page 12 and Figure 2 on page 12.

Signal	I/O	Description
VSSP	G	**PLL Ground.** Should be connected to a digital ground plane via a 0Ω resistor.
VPLL18	P	**PLL 1.8V Supply.** Internally generated for PLL. Should be connected via a 4.7 μF ceramic capacitor to VSSP.
VD18	P	**Internal 1.8V Supply.** Internally generated for internal logic. Should be connected via a 4.7 μF ceramic capacitor to digital ground.
VSS	G	**Digital Ground.** Should be connected to a digital ground plane. The QFN32 package bottom pad must be connected to digital ground.
VDD	P	**3.3V Digital Supply.**

1.3.6 Not Connected

Signal	I/O	Description
NC		**Not Connected.** Should be left open and not be connected to any signal.

2.0 Power, Clocks and Reset

2.1 POWER

2.1.1 Power Planes

The NPCA110D has three power plane groups (wells), as shown in Table 3.

Table 3. NPCA110D Power Planes

Power Plane Group	Description	Power Plane Notation	Power Pins	Ground Pins
Internal group	Powers the internal PLL. Supply is generated internally, but requires filtering.	V_{D18}	VPLL18	VSSP
	Powers the internal logic of all the device modules. Supply is generated internally but requires filtering.	V_{D18}	VD18	VSS
Active group	3.3V power to the I/O interface and internal regulator.	V_{DD}	VDD	VSS

2.1.2 Power States

The NPCA110D has the following main power states:

- **Power Fail**
  All power planes are powered off; (i.e., V_{DD} inactive).
- **Power Active**
  All power planes are powered on (i.e., V_{DD} active).

Illegal Power States

The following power states are illegal (i.e., NPCA110D operation is not guaranteed):

- Active power plane on and analog power plane off.
- Active power plane off and analog power plane on.

2.1.3 Power Connection and Layout Guidelines

The NPCA110D requires a power supply voltage of 3.13V–3.47V for the digital supplies (V_{DD}).

V_{DD} uses a common ground return named Digital Ground and marked V_{SS}. The analog circuits use a separate ground return. This ensures effective isolation of the analog modules from noise caused by the digital modules.

The following directives are recommended for the NPCA110D power and ground connections.

Ground Connection

Use a plane for digital signals (VSS). Make the following ground connections:

- Connect all VSS pins and the bottom pad of the NPCA110D to the GND plane.
- Locate the decoupling capacitors of the Active power plane's digital supply (VDD) pins close to a VDD pin; connect one terminal of each capacitor to the ground plane.
- If there is insufficient room for decoupling capacitors, place smaller capacitors close to the power-ground pins and larger capacitors further away.

Note that low-impedance ground layers improve noise isolation and reduce ground bounce problems.

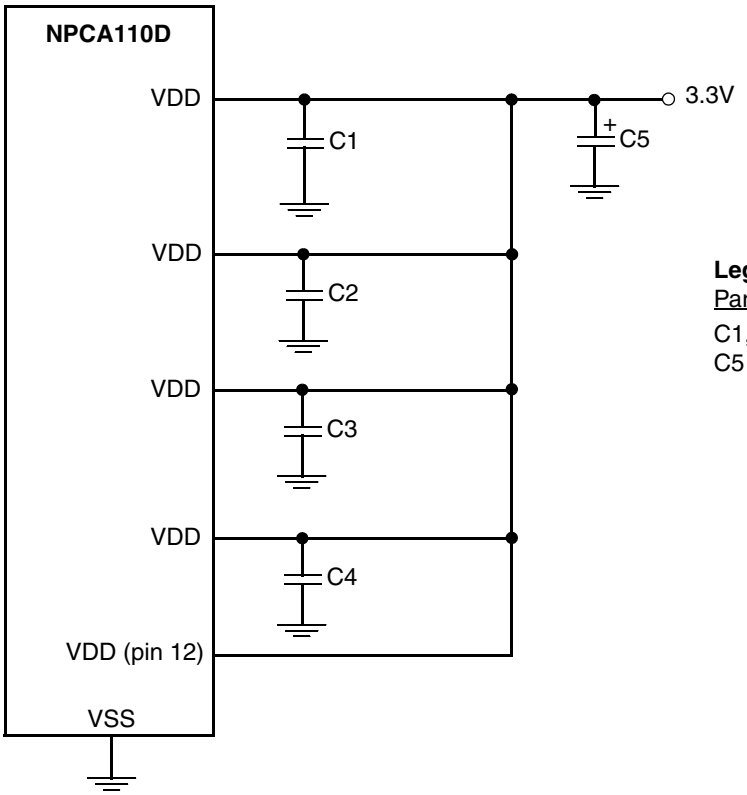
Power Connection

All NPCA110D supply pins must be connected to the appropriate power plane. Decoupling capacitors must be used as recommended as follows:

- Connect the digital supply pins (VDD) to a 3.3V power supply. A 10 μF (or larger) capacitor should be connected between VDD and the digital ground plane. A 0.1μF capacitor should be connected to ground near each VDD pin of the device.

The recommend power connections are shown below:

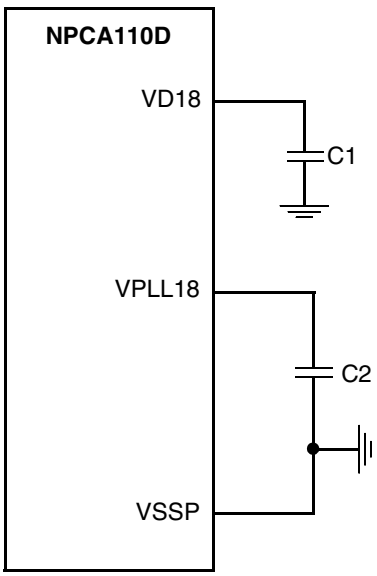
2.0 Power, Clocks and Reset (Continued)



Legend:

Part Designator	Value
C1, C2, C3, C4	0.1 µF Ceramic
C5	10 µF (for linear regulator), 22 µF (for switching regulator)

Figure 1. 3.3V Digital Power Connection Diagram

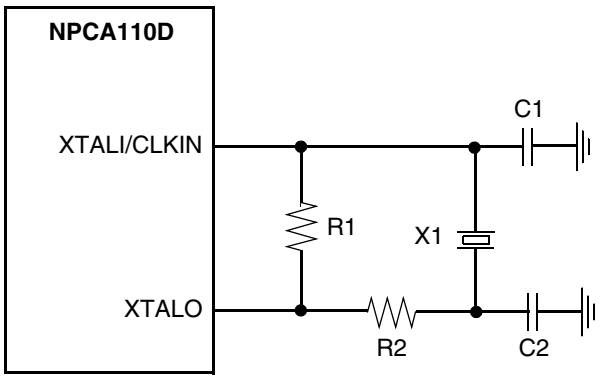


Legend:

Part Designator	Value
R1	0Ω
C1, C2	4.7 µF Ceramic

Figure 2. 1.8V Power Connection Diagram

2.0 Power, Clocks and Reset (Continued)



Legend:

Part Designator	Final Values
R1	2 MΩ 5%,
C1	20 pF Ceramic 5%,
C2	20 pF Ceramic 5%
Option 1:	
R2	2000Ω 1%,
X1	12.288 or 11.2896 MHz, C_L=12 pF, ESR < 75Ω, Drive level up to 500 µW
Option 2:	
R2	4990Ω 1%,
X1	12.288 or 11.2896 MHz, C_L=12 pF, ESR < 75Ω, Drive level up to 100 µW

Figure 3. Typical Crystal Oscillator Connection Diagram

2.0 Power, Clocks and Reset (Continued)

2.2 CLOCKS

The NPCA110D clock structure is shown below. The clock generation parameters are supplied to the device at initialization.

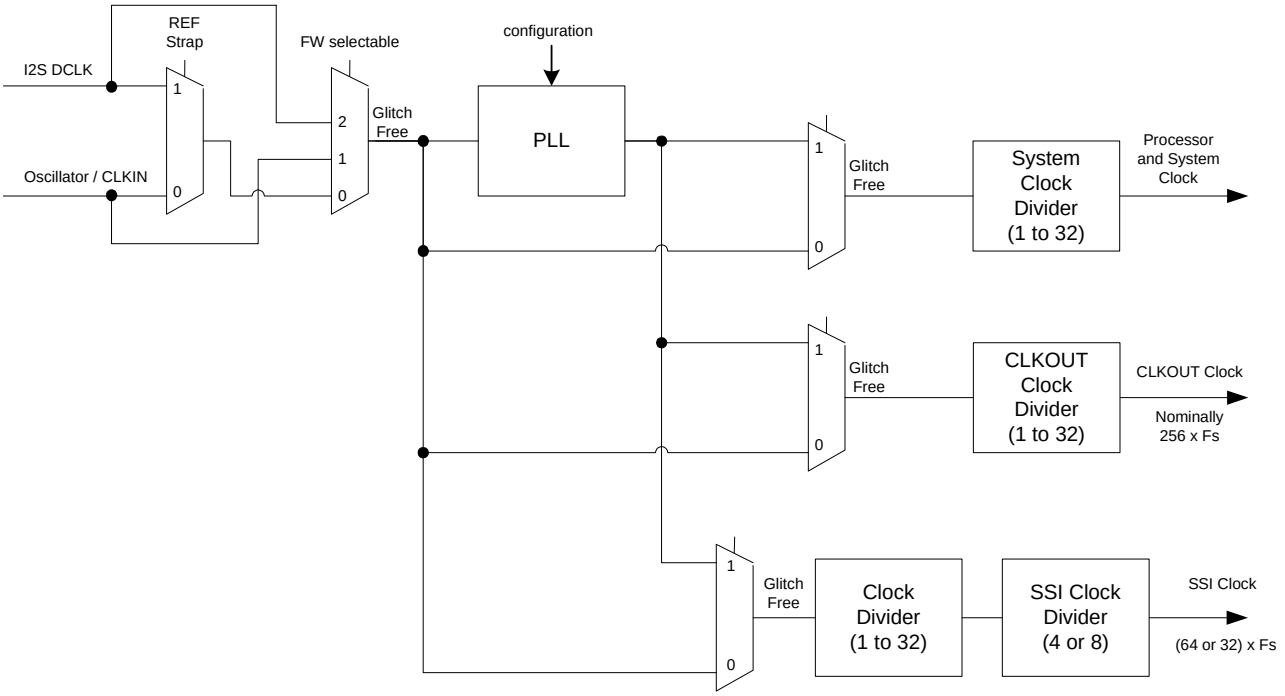


Figure 4. Clocks in the NPCA110D

Clock Source

The clock source is either DCLK (I2S serial clock, in slave mode) or the crystal oscillator, and is used as the reference clock of the PLL. The clock is selected initially by the REF strap and may be changed later.

When DCLK is a stable clock, the oscillator may be omitted. The oscillator may be replaced by a clock input.

The best selection for a crystal frequency is 256 times the sample clock used.

PLL

The PLL is used to generate the Processor clock and can be used to generate the SSI (I2S) clock as well (if the device is in I2S master mode).

The PLL reference clock may be as low as 44 KHz; however, for low jitter, a higher frequency reference clock is recommended.

2.0 Power, Clocks and Reset (Continued)

2.3 RESET SOURCES AND TYPES

The NPCA110D has one reset domain.

Reset Types

- Power-Up reset - Activated when nReset signal is asserted (when the V_{DD} and V_{D18} supplies are powered up).
- Watchdog reset - Activated when a watchdog condition is detected.

The following sections describe the sources and effects of the various resets on the NPCA110D, per reset type.

2.3.1 Power-Up Reset

V_{DD} Power-Up reset is generated when nRESET signal is asserted.

On Power-Up reset, the NPCA110D performs the following:

- Puts pins with strap options into TRI-STATE® mode and enables the internal pull-up/down resistors on the strap pins.
- Samples the values of the strap pins (after nRESET deassertion).
- Performs all actions done by a Watchdog reset.

Note: The internal reset signal is active for at least 3 ms.

2.3.2 Watchdog Reset

Watchdog reset is generated by the Watchdog module on detection of a watchdog event.

The NPCA110D loads default values to all registers.

3.0 Device Specifications

3.1 GENERAL DC ELECTRICAL CHARACTERISTICS

3.1.1 Recommended Operating Conditions

Symbol	Parameter[1]	Min	Typ	Max	Unit
V_{DD}	3.3V Supply Voltage (VDD pins)	3.13	3.3	3.47	V
V_{OFF}	V_{DD} Power Off Voltage	–0.3	0	+0.5	V
T_A	Operating Ambient Temperature	0		+70	°C

1. Unless otherwise specified, all voltages are relative to ground.

3.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground. These parameters are characterized and not fully tested.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	3.3V Supply Voltage[1]		–0.5	3.6	V
V_I	Input Voltage[1]	All buffer types (except analog)	–0.5	V_{DD} + 0.5	V
		5V buffer types	–0.5	5.5	V
		V_{DD} < 0.5V, all digital signals	–0.5	3.47	V
V_O	Output Voltage[1]	All buffer types (except analog)	–0.5	V_{DD} + 0.5	V
I_{SINK}	Total NPCA110D Sink or Source Current	Total of all output pins		50	mA
	ESD Tolerance	C_{ZAP} = 100 pF, R_{ZAP} = 1.5 KΩ[2]	2000		V
T_{STG}	Storage Temperature		–65	+150	°C
T_{BIAS}	Ambient Temperature Under Bias		0	+70	°C
P_D	Power Dissipation	For correct operation		0.5	W

1. All voltages are relative to ground.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

3.1.3 Capacitance

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Unit
C_{IO}	I/O Pin Capacitance	All pins		8	12	pF

1. Not fully tested; characterized only.
2. T_A = 25°C; f = 1 MHz.

3.0 Device Specifications (Continued)

3.1.4 Power Supply Current Consumption under Recommended Operating Conditions

These table values are preliminary:

Symbol	Parameter	Power Mode	Conditions[1]	Typ[2]	Max[2]	Unit
I_{DD}	V_{DD} Average Supply Current	Active	V_{IL} = 0.5V, V_{IH} = 2.4V, Processor clock is 125 MHz	44	59	mA
I_{DD}	V_{DD} Stop[3] Supply Current	Idle		0.7		mA

1. Unless stated otherwise, all parameters are specified for 0°C ≤ T_A ≤ 70°C, V_{33} = 3.13V - 3.47V and no resistive load on outputs.
2. Not fully tested; characterized only.
3. Stop is defined as: Processor and system clock is halted, PLL is in power-down (Reference clock selected as clock, PLLPD bit set, crystal oscillator disabled).

3.2 DC CHARACTERISTICS OF PINS BY I/O BUFFER TYPES

The tables in this section summarize the DC characteristics of all device pins described in (Section 1.3 on page 8). The characteristics describe the I/O buffer types defined in Section 1.2 on page 8. For exceptions, see Section 3.2.5 on page 18.

3.2.1 Input, TTL Compatible

Symbol: T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage	Non-5V types	2.0	V_{DD}+0.5	V
		5V types	2.0	5.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
I_{ILK}[1]	Input Leakage Current	V_{DD} = 3.13V – 3.47V and 0 < V_{IN} < V_{DD}		±2	µA

1. For additional conditions, see Section 3.2.5 on page 18.

3.2.2 Input, TTL Compatible, with Schmitt Trigger

Symbol: ST

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage	Non-5V types	2.0	V_{DD}+0.5	V
		5V types	2.0	5.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_H	Input Hysteresis		280[1]		mV
I_{ILK}[2]	Input Leakage Current	V_{DD} = 3.13V – 3.47V and 0 < V_{IN} < V_{DD}		±2	µA

1. Not tested; guaranteed by characterization guardband.
2. For additional conditions, see Section 3.2.5 on page 18.

3.0 Device Specifications (Continued)

3.2.3 Output, TTL/CMOS-Compatible, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL/CMOS-compatible, rail-to-rail push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -p$ mA	2.4		V
		$I_{OH} = -50$ µA	$V_{DD} - 0.2$		V
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V
		$I_{OL} = 50$ µA		0.2	V
I_{OLK}[1]	Output Leakage Current	$V_{DD} = 3.13V - 3.47V$ and $0 < V_{IN} < V_{DD}$		±2	µA

1. For additional conditions, see Section 3.2.5 on page 18.

3.2.4 Output, TTL/CMOS-Compatible, Open-Drain Buffer

Symbol: OD_n

Output, TTL/CMOS-compatible open-drain output buffer capable of sinking *n* mA. Output from these signals is open-drain and is never forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V
		$I_{OL} = 50$ µA		0.2	V
I_{OLK}[1]	Output Leakage Current	$V_{DD} = 3.13V - 3.47V$ and $0 < V_{IN} < V_{DD}$		±2	µA

1. For additional conditions, see Section 3.2.5 on page 18.

3.2.5 Notes and Exceptions

1. I_{ILK} and I_{OLK} are measured in the following cases (where applicable):
   - Internal pull-up or pull-down resistor is disabled
   - Push-pull output buffer is disabled (TRI-STATE mode)
   - Open-drain output buffer is at high level
2. Pins marked with '5V' in the Buffer Type column in Section 1.3 on page 8 are 5V tolerant.
   The analog type pins, are not 5V tolerant. This applies if these buffer types are stand-alone or if they are multiplexed with 5V tolerant buffer types.
3. Maximum leakage of all the NPCA110D pins together is <10 µA when input voltage is within the supply rails voltage and when PU resistors are disabled in Hi-Z (not fully tested; characterized only).
4. A pin (nRESET) that has an internal static pull-up resistor therefore has leakage current from V_{DD} (when $V_{IN} = 0$).
5. Strap pins have an internal pull-up resistor enabled during Power-Up reset and therefore may have leakage current from V_{DD} (when $V_{IN} = 0$).
6. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
7. All digital pins of output type $O_{p/n}$ have a back-drive protection capability of up to 3.6V.

3.2.6 Terminology

Back-Drive Protection. Back-drive protected pins sustain any voltage within the specified voltage limits when the device power supply is off.

5-Volt Tolerance. 5V tolerant pins sustain 5V even if the applied voltage is above the device power supply voltage. A pin is 5V tolerant in the following conditions (where applicable):

- Internal pull-down resistor is disabled. If it is enabled, leakage current is high.
- Push-pull output buffer is disabled (TRI-STATE mode)

3.0 Device Specifications (Continued)

3.3 INTERNAL RESISTORS

DC Test Conditions

Pull-Up Resistor Test Circuit

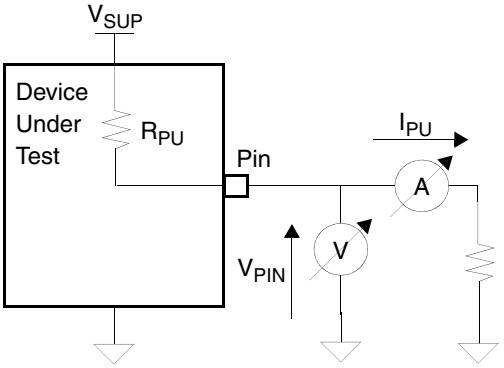


Figure 5. Internal Resistor Test Conditions, T_A = 0°C to 70°C

Internal Pull-Up Strap

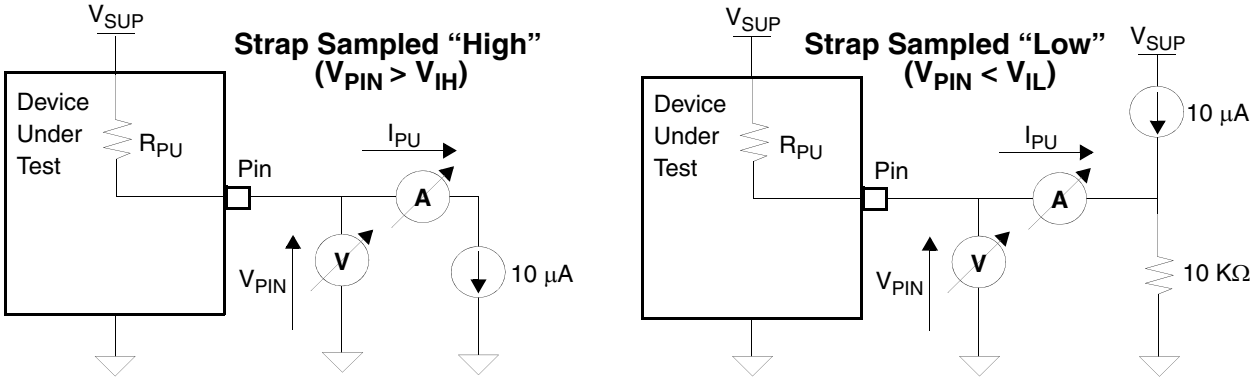


Figure 6. Internal Resistor Design Requirements, T_A = 0°C to 70°C

Notes:
1. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
2. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

3.3.1 Pull-Up Resistors

Symbol: PU

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-Up Equivalent Resistance for other pins	V_{PIN} = 0V	34	60	95	KΩ

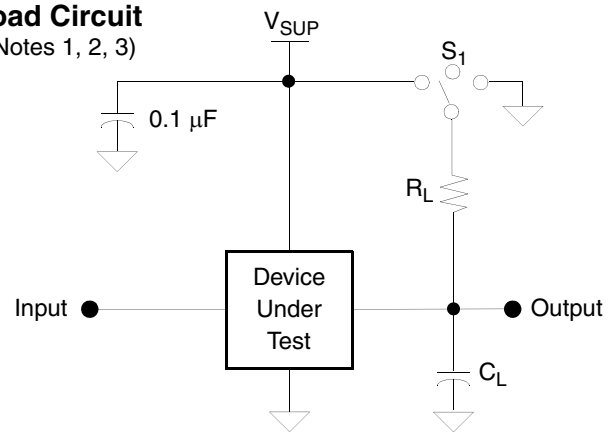
1. TA = 0°C to 70°C, V_{SUP} = 3.3V ±5%.
2. Not fully tested; characterized only.

3.0 Device Specifications (Continued)

3.4 AC ELECTRICAL CHARACTERISTICS

3.4.1 AC Test Conditions

Load Circuit
(Notes 1, 2, 3)



AC Testing Input, Output Waveform

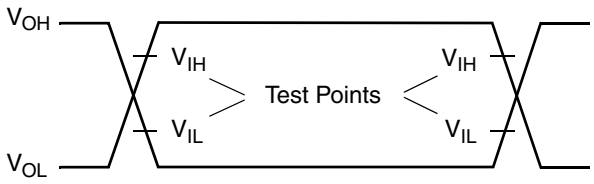


Figure 7. AC Test Conditions, T_A = 0°C to 70°C, V_{SUP} = 3.13V - 3.47V

Notes:

1. V_{SUP} is V_{33} according to the power well of the pin, relevant for all signals at LVTTL levels.
2. C_L = 50 pF for all output pins except the following pin groups (values include both jig and oscilloscope capacitance)
   C_L = 100 pF for I2C
   C_L = as otherwise defined
3. S_1 = Open – for push-pull output pins
   S_1 = V_{SUP} – for high-impedance to active low and active low to high-impedance transition measurements
   S_1 = GND – for high-impedance to active high and active high to high-impedance transition measurements
   R_L = 1.0 KΩ – for all pins
4. The following abbreviations are used in Section 3.4: RE = Rising Edge; FE = Falling Edge.

Definitions

The timing specifications in this section are relative to V_{IL} or V_{IH} (according to the specific buffer type) on the rising or falling edges of all the signals, as shown in the following figures (unless specifically stated otherwise).

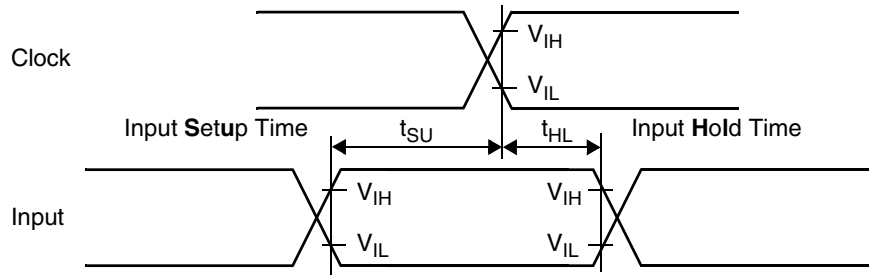


Figure 8. Input Setup and Hold Time

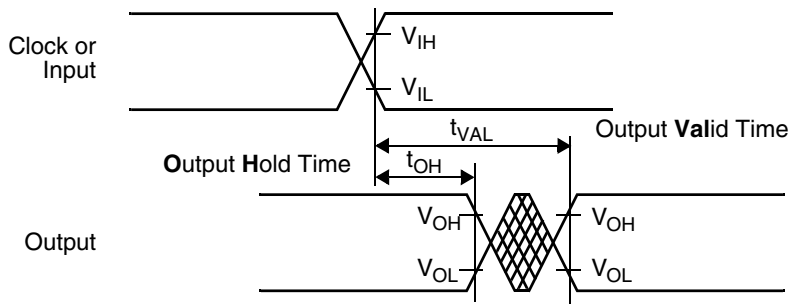


Figure 9. Clock-to-Output and Propagation Delay

3.0 Device Specifications (Continued)

3.4.2 Reset Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
t_{CORD}	10	Power-Up Requirement: all power supplies at valid level until nRESET deasserted[1]	After reset delay	5		ms
t_{PRST}	10	nRESET Pulse Width	To assure reset	1		ms
t_{RSTC}	10	Internal reset delay after nRESET deasserted	REF latched high	11000	12500	t_{REFCLK}
			REF latched low	48000	52000	t_{REFCLK}
$t_{CLKRSTD}$	10	Stable reference clock to reset end		100		µs
t_{STSU}	10	Valid straps signals level setup time to nRESET rising		100		µs
t_{STH}	10	Valid straps signals level hold after nRESET rising		10		t_{REFCLK}
t_{OE}	10	Internal reset end to outputs enabled on strap pins		-100		t_{REFCLK}

1. Requirement for system.

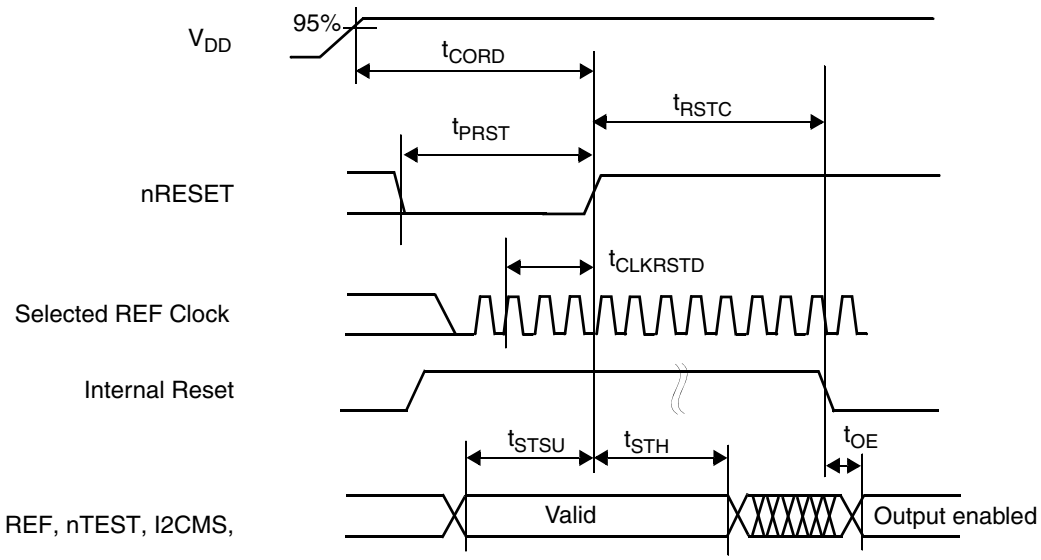


Figure 10. Device Reset

3.0 Device Specifications (Continued)

3.4.3 Clock Timing

CLKREF (DCLK or Oscillator) Clock Timing

Symbol	Figure	Description	Conditions	Min	Typ	Max	Units
t_{REFCLK}	11	CLKREF Average Clock Period	From RE to RE of CLKREF	50		1000	ns
A_{CLK}		CLKREF Accuracy	For a specific system		50	100	ppm
t_{CLKH}	11	CLKREF High Time	From RE to FE of CLKREF	35			ns
t_{CLKL}	11	CLKREF Low Time	From FE to RE of CLKREF	35			ns
t_{CLKR}	11	CLKREF Rise Time	From 0.8V to 2.0V			5	ns
t_{CLKF}	11	CLKREF Fall Time	From 2.0V to 0.8V			5	ns
Duty Cycle		CLKREF Duty Cycle	At 1.4V	40		60	%
J_{PERIOD}		Period Jitter[1]	At 1.4V			1.5	ns

1. Measured over a 20 µs window.

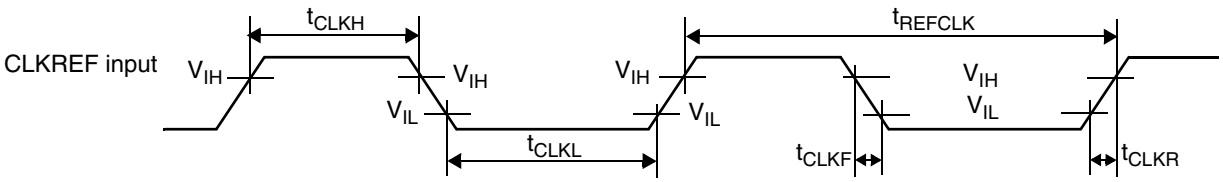


Figure 11. CLKREF Clock Waveforms

CLKOUT Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
t_{CLK}	12	CLKOUT Clock Period	From RE to RE of CLKOUT, C_L = 20 pF	50		ns
t_{CLKH}	12	CLKOUT High Time[1]	From RE to FE of CLKOUT, C_L = 20 pF	15		ns
t_{CLKL}	12	CLKOUT Low Time[1]	From FE to RE of CLKOUT, C_L = 20 pF	15		ns
t_{CLKR}	12	CLKOUT Rise Time[1]	From V_{IL} to V_{IH} of CLKOUT, C_L = 20 pF		5	ns
t_{CLKF}	12	CLKOUT Fall Time[1]	From V_{IH} to V_{IL} of CLKOUT, C_L = 20 pF		5	ns
D_{CLK}		CLKOUT Duty Cycle[1]	C_L = 20 pF	28		%

1. Not fully tested; characterized only.

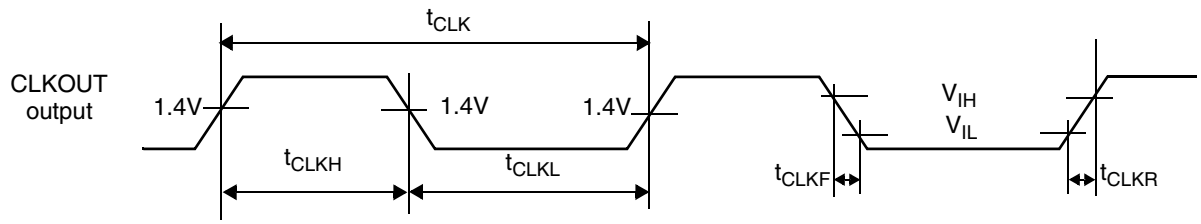


Figure 12. CLKOUT Clock Waveforms

3.0 Device Specifications (Continued)

3.4.4 Input Signals Detection Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
t_{SSCL}	13	Debounced SCL input pulse width (which guarantees detection)		15		ns

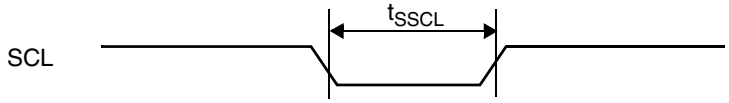


Figure 13. Input Signal Detection Timing

3.4.5 I2C Slave Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
f_{SCL}	14	SCL Frequency	At 1.2V SCL RE to RE		400[1]	KHz
t_{LOW}		SCL Low Time	At 0.8V (both edges)	0.5		µs
t_{HIGH}	14	SCL High Time	At 2.0V (both edges)	0.26		µs
t_{I2CR}	14	SCL, SDA Rise Time	From 0.8V to 2.0V[1]		0.25[2]	µs
t_{I2CF}	14	SCL, SDA Fall Time	From 2.0V to 0.8V[1]		100	ns
$t_{SU:DAT}$	14	SDA Setup Time	Before SCL RE	50		ns
$t_{HD:DAT}$	15	SDA Hold Time	After SCL FE	18		ns
$t_{SU:STA}$	15	SCL Setup Time	Before Restart condition	0.26		µs
$t_{HD:STA}$	15	SCL Hold Time	After Start/Restart condition	0.26		µs
$t_{SU:STO}$	15	SCL Setup Time	Before Stop condition	0.26		µs
t_{BUF}	15	Bus Free Time	Between Stop and Start conditions	0.5		µs
$t_{VD:DAT}$	15	Data Valid Time	After SCL FE		0.45	µs
$t_{VD:ACK}$	15	Data Valid Acknowledge Time	After SCL FE		0.45	µs

1. Test conditions: R_L = 1 KΩ to V_{DD} = 3.3V, C_L = 100 pF to GND
2. Not tested; based on design simulation.

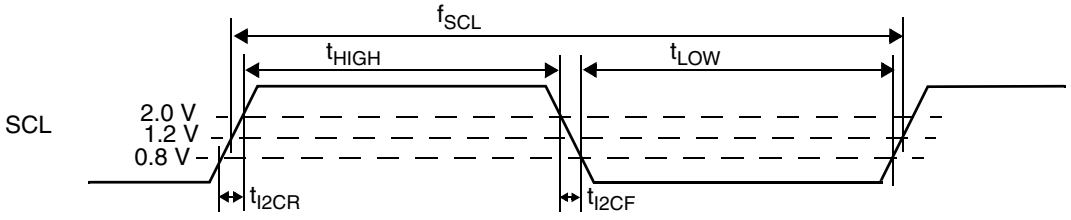


Figure 14. I2C SCL Signal Timing

3.0 Device Specifications (Continued)

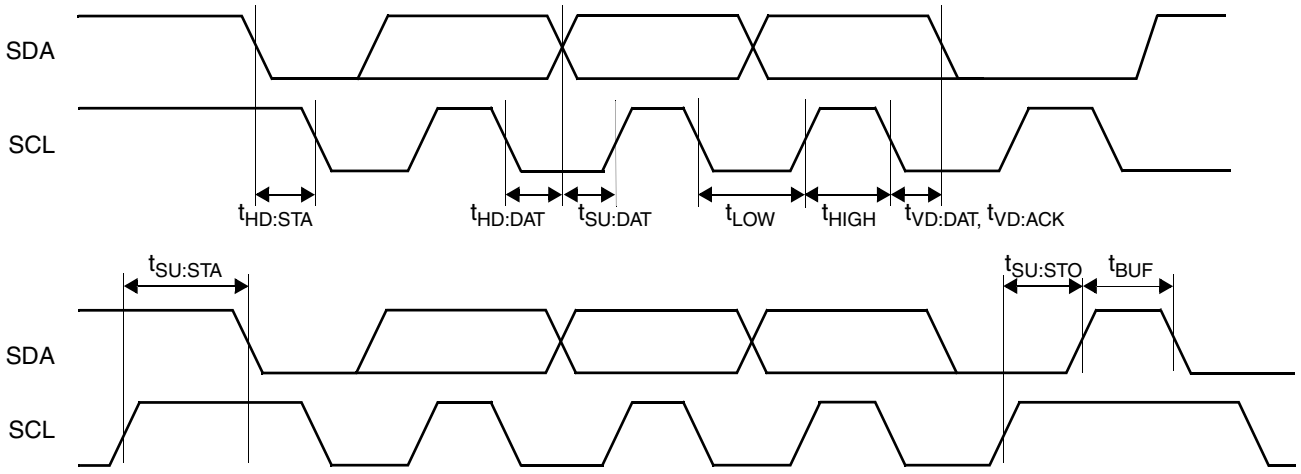


Figure 15. I2C Timing

3.4.6 I2C Master Timing

Symbol	Figure	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	14	SCL Frequency[4]	Programming capability	f_{AEE} / 16384		f_{AEE} / 8	
		SCL Frequency[4]	At 1.2V SCL RE to RE	0		400 [1]	KHz
t_{LOW}	14	SCL Low Time[4]	At 0.8V (both edges)	8 x T_{AEE}[2]	0.5 x T_{SCL}[3]		
t_{HIGH}	14	SCL High Time[4]	At 2.0V (both edges)	8 x T_{AEE}	0.5 x T_{SCL}		
t_{I2CR}	14	SCL, SDA Rise Time	From 0.8V to 2.0V[1]			0.25[4]	µs
t_{I2CF}	14	SCL, SDA Fall Time[4]	From 2.0V to 0.8V[1]			100	ns
$t_{SU:DAT}$	15	SDA Setup Time[4]	Before SCL RE	4 x T_{AEE}	0.25 x T_{SCL}		
$t_{HD:DAT}$	15	SDA Hold Time[4]	After SCL FE	4 x T_{AEE}	0.25 x T_{SCL}		
$t_{SU:STA}$	15	SCL Setup Time[4]	Before Restart condition	12 x T_{AEE}	0.5 x T_{SCL}		
$t_{HD:STA}$	15	SCL Hold Time[4]	After Start/Restart condition	4 x T_{AEE}	0.5 x T_{SCL}		
$t_{SU:STO}$	15	SCL Setup Time[4]	Before Stop condition	4 x T_{AEE}	0.5 x T_{SCL}		
t_{BUF}	15	Bus Free Time[4]	Between Stop and Start conditions	16 x T_{AEE}	0.5 x T_{SCL}		
$t_{VD:DAT}$	15	Data Valid Time[4]	After SCL FE	4 x T_{AEE}	0.5 x T_{SCL}		
$t_{VD:ACK}$		Data Valid Acknowledge Time[4]	After SCL FE	4 x T_{AEE}	0.5 x T_{SCL}		

1. Test conditions: R_L = 1 KΩ to V_{DD} = 3.3V, C_L = 100 pF to GND.
2. T_{AEE} is the Processor core clock period.
3. T_{SCL} is the SCL clock period ($1/f_{SCL}$).
4. Not tested; based on design simulation.

3.0 Device Specifications (Continued)

3.4.7 SSI Timing

Symbol	Figure	Description	Conditions	Min	Typ	Max	Units
t_T	16	DCLK Cycle Time	At 1.3V DCLK RE to RE	1/64	1/64	1/32	$1/F_S$ [1]
f_{DCLK}		DCLK Frequency		32	64	64	F_S [1]
t_{LOW}	16	DCLK Low Time	At 0.8V (both edges)	0.35	0.5		t_T
t_{HIGH}	16	DCLK High Time	At 2.0V (both edges)	0.35	0.5		t_T
t_{HTR}	16	Output Hold Time	After DCLK RE	15 ns	0.5 * t_T		
t_{DTR}	16	Output Valid Time	After DCLK RE		0.5	0.75	t_T
t_{HR}	16	Input Hold Time	After DCLK RE	2			t_T
t_{SR}	16	Input Setup Time	Before DCLK RE	0.2			t_T

1. F_S is the audio sampling frequency

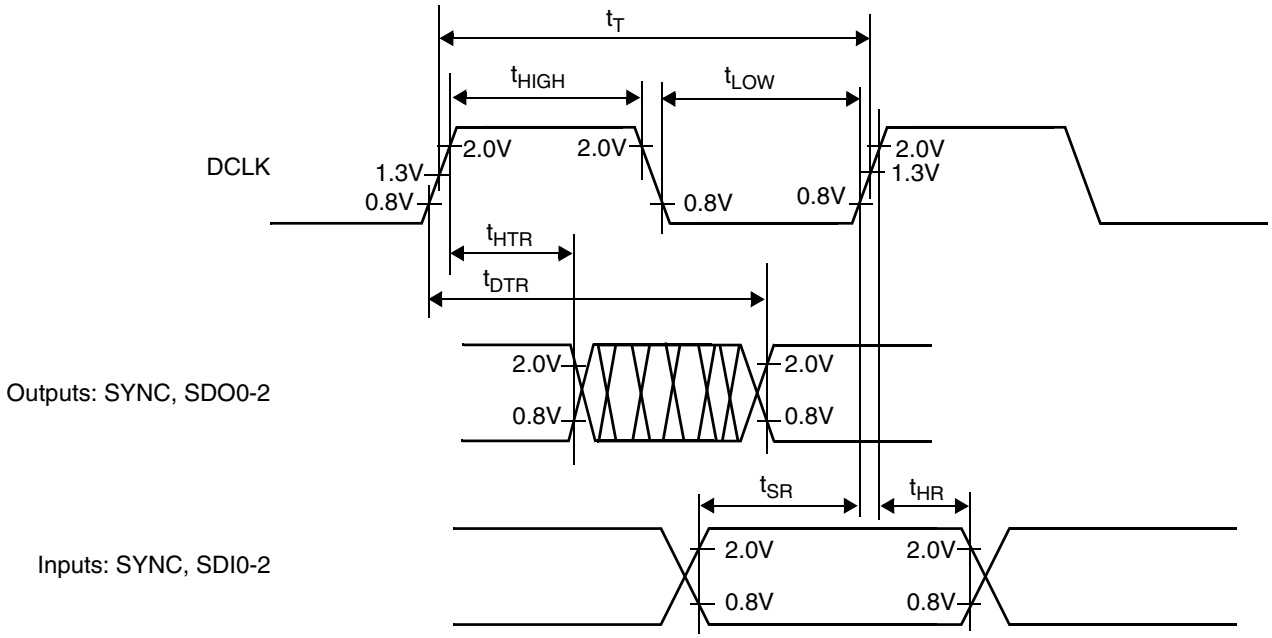


Figure 16. SSI Signal Timing

3.0 Device Specifications (Continued)

3.5 PACKAGE THERMAL INFORMATION

Thermal resistance (degrees ^{o}C/W) $Theta_{JA}$ values for the NPCA110D packages are as follows:

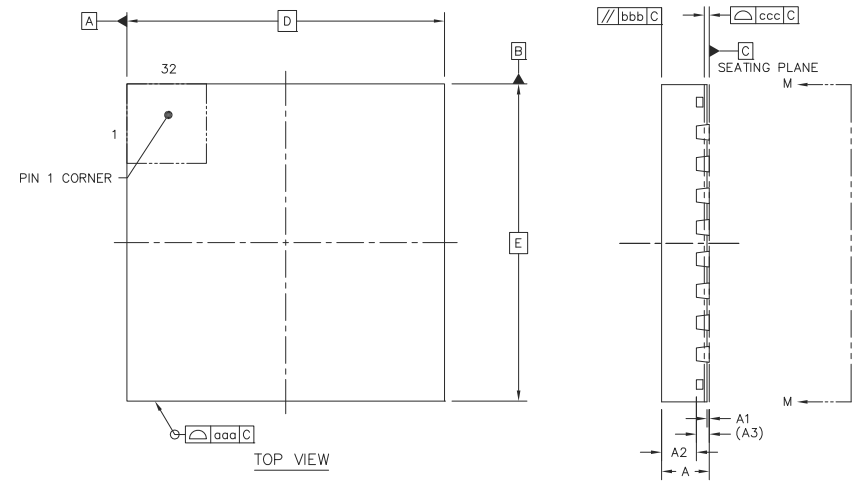
Table 4. Theta (Θ) J-A Values

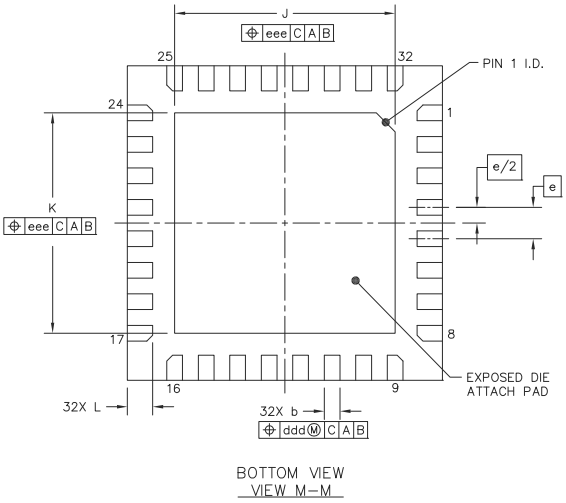
	Θ_{JA} (Degrees Kelvin/Watt)		
Package	**0 m/s**	**1 m/s**	**2 m/s**
32-Pin QFN32	54	46	45

Note: All values apply to a device soldered to a 4-layer PCB.

Physical Dimensions

Control dimensions are in millimeters.





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

32-Pin Quad Flat No-Lead (QFN) Package
Order Number: NPCA110DA0YX

Device topside mark specification:

1st Line: Part number - NPCA110D
2nd Line: A0YX YWW.
A0 - End of part number; 'Y': QFN package indicator;
'X': Green package finish indicator.
YWW: Date Code.
3rd and 4th Lines: Nuvoton proprietary information.

Date code: YWW, where Y is the year and WW is the week. For example, date code 035 indicates that device assembly was done on week 35, year 2010.

NPCA110D
A0YX YWW
ZZ ZZZZZZ
ZZZZZ

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