1T 8051

8-bit Microcontroller

NuMicro® Family
ML51 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The ML51 is a Flash embedded 1T 8051-based microcontroller. The instruction set of the ML51 is fully compatible with the standard 80C51 with performance enhanced and low power consumption.

The ML51 runs up to 24 MHz at a wide voltage range from 1.8V to 5.5V, and contains up to 64/32/16/8 Kbytes Flash called APROM for programming code. The ML51 Flash supports In-Application-Programming (IAP) function, which enables on-chip firmware updates. Partial Flash can be optionally configured as Data Flash programmed by IAP and read by IAP or MOVC instruction. The ML51 includes an additional configurable up to 4/3/2/1 Kbytes Flash area called LDROM, in which the Boot Code normally resides for carrying out the In-System-Programming (ISP). To facilitate mass production programming and verification, the Flash is allowed to be programmed and read electronically by parallel Writer/Programmer or In-Circuit-Programming (ICP) with Nu-Link. Once programmed and verified, the programmed code can be protected by the flash lock mechanism for not being read out by any external programming tool.

The ML51 provides rich peripherals including 256 bytes of SRAM, 4/2/1 Kbytes of auxiliary RAM (XRAM), up to 43 general purpose I/O, two 16-bit Timers/Counters 0/1, one 16-bit Timer2 with three-channel input capture module, one Watchdog Timer (WDT), one Self Wake-up Timer (WKT), one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, two ISO7816 Smartcard interface, two SPI, two I^2C, 12 enhanced PWM output channels with dead zone control, two analog comparators, eight-channel shared pin interrupt for all I/O ports, and one 12-bit ADC at 500 ksps. There are a total of 30 sources with 4-level-priority interrupts capability.

The ML51 is equipped with four clock sources and supports on-the-fly clock switching via software control. The four clock sources include two sets of external crystal inputs (HXT, LXT), 38.4 kHz internal oscillator, and one 24 MHz internal high-precision ±5% oscillator. The ML51 provides additional power monitoring detection such as power-on reset and 7-level brown-out detection, which stabilizes the power-on/off sequence for a high reliability system design.

The ML51 microcontroller provides 3 power modes to reduce power consumption —Low power run mode, Low power Idle mode, and Power down mode. In Low power run mode, the power consumption can be down to 15 uA at 38.4 kHz LIRC. In Low power idle mode, CPU processing is suspended by holding the Program Counter. No program code is fetched and run in low power idle mode if the power consumption does not exceed 13 uA. Power down mode stops the whole system clock for minimum power consumption with the leakage current less than 1 uA. The system clock of the ML51 can also be slowed down by software clock divider, which allows for flexibility between execution performance and power consumption.

Through the high performance of 1T 8051 core, low power performance of ML51 and rich well-designed peripherals, the ML51 benefits for low-power, battery powered devices, general purpose, home appliances, or motor control system.

2 FEATURES

- CPU:
  - Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller.
  - Instruction set fully compatible with MCS-51.
  - 4-priority-level interrupts capability.
  - Dual Data Pointers (DPTRs).
- Operating:
  - Wide supply voltage from 1.8 V to 5.5 V.
  - Wide operating frequency up to 24 MHz
  - Industrial temperature grade: -40 ℃ to +105 ℃.
- Low power features:
  - Normal run typical power consumption 80μA /MHz
  - Low power run mode typical power consumption 15 μA
  - Low power Idle mode power consumption does not exceed 13 μA
  - Power down mode typical power consumption less than 1 μA
  - Wake up time from power down mode less than 10 μs (run with HIRC).
- Memory:
  - Up to 64/32/16 Kbytes of APROM for User Code.
  - 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP)
  - Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP).
  - Flash Memory 100,000 writing cycle endurance.
  - Code lock for security.
  - 256 Bytes on-chip RAM.
  - Additional 4/2/1 Kbytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
- PDMA:
  - Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer.
  - Source address and destination address must be word alignment in all modes.
  - Memory-to-memory mode: transfer length must be word alignment.
  - Peripheral-to-memory and memory-to-peripheral mode: transfer length could be byte alignment.

  - Peripheral-to-memory and memory-to-peripheral mode: transfer data width byte alignment.

- Clock sources:
  - 24 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 ℃, 3.3 V), ±5% in all conditions.
  - 38.4 kHz low-speed internal oscillator (LIRC) calibrating to ±2% by software from high-speed internal oscillator (HIRC) or external crystal (HXT).
  - External 4~24 MHz crystal (HXT) input for precise timing operation.
  - External 32.768 kHz (LXT) crystal input.
  - On-the-fly clock source switch via software.
  - Programmable system clock divider from 1/2, 1/4, 1/6, 1/8…, up to 1/512.
- Peripherals:
  - Up to 43 general purpose I/O pins. All output pins have individual 2-level slew rate control.
  - 8 channels of GPIO interrupt with variable edge/level detection from all 43 GPIO configure as one of the input source.
  - Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$ compatible with standard 8051.
  - Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.
  - One 16-bit Timer 2 with three-channel input capture module.
  - One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.
  - One programmable Watchdog Timer (WDT) clocked by dedicated 38.4 kHz LIRC.
  - One dedicated Self Wake-up Timer (WKT) for self-timed wake-up for power reduced modes by dedicated 38.4 kHz LIRC or 32.768 kHz LXT.
  - Two full-duplex UART ports with frame error detection and automatic address recognition.
  - Two smart card port supports ISO7816-3 compliant T=0, T=1 and supports full-duplex UART mode .
  - Two SPI port with master and slave modes, up to 6 Mbps when system clock is 24 MHz
  - Two I^2C bus with master and slave modes, up to 400 kbps data rate.
  - 6 pairs, 12 channels of pulse width modulator (PWM) output, up to 16-bit resolution, with different modes and Fault Brake function for motor control. The 16-bit PWM counter individual used as timer with interrupt.
  - Two comparator supports hysteresis function.
  - One 12-bit ADC, up to 500 ksps (when V_{DD} over then 2.5 V) converting rate, hardware triggered and conversion result compare facilitating motor control.
- Power monitor:

  - Brown-out detection (BOD) with low power mode available, 7-level selection, interrupt or reset options.
  - Power-on reset (POR).
  - Low voltage reset (LVR).
- Strong ESD and EFT immunity.
  - ESD HBM pass 8 kV
  - EFT > ± 4.4 kV
  - Latch-up pass 150 mA
- Development Tools:
  - Nuvoton Nu-Link with KEIL™ and IAR development environment.
  - Nuvoton In-Circuit-Programmer (Nu-Link).
  - Nuvoton In-System-Programming (ISP) via UART.

3 PARTS INFORMATION

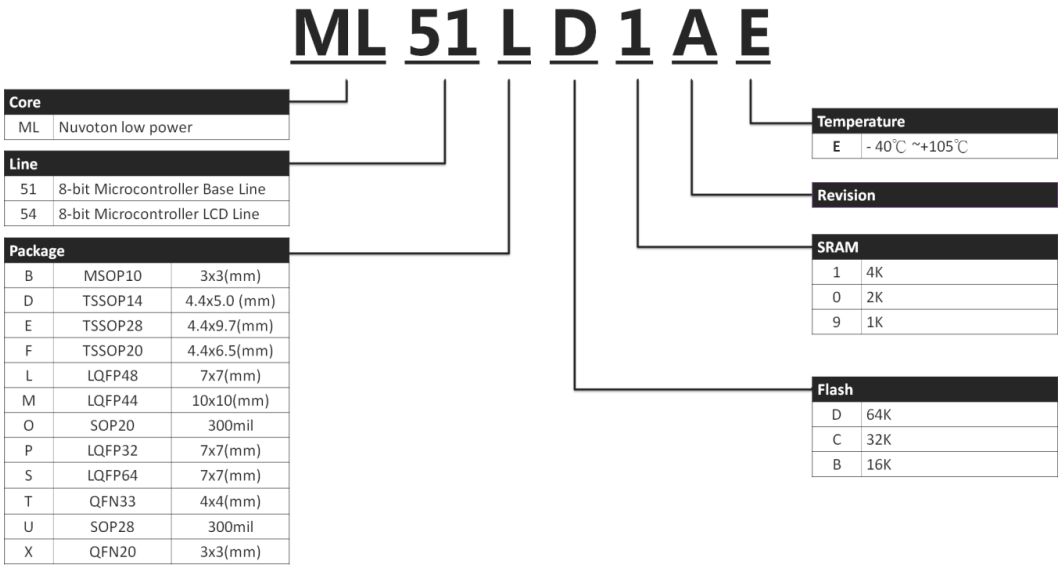
3.1 ML51 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)*	I/O	Timer/	PWM	Analog Comparator	Internal Voltage Reference	PDMA	Connectivity				ADC(12-Bit)	Package
										ISO-7816**	UART	SPI	I2C		
ML51BB9AE	16	1	4*	7	4	6	-	-	-	1	2	1	2	2-ch	MSOP10
ML51DB9AE	16	1	4*	11	4	6	-	-	-	1	2	1	2	3-ch	TSSOP14
ML51FB9AE	16	1	4*	16	4	6	-	-	-	1	2	1	2	6-ch	TSSOP20
ML51OB9AE	16	1	4*	16	4	6	-	-	-	1	2	1	2	6-ch	SOP20
ML51XB9AE	16	1	4*	17	4	5	-	-	-	1	2	1	2	6-ch	QFN20
ML51EB9AE	16	1	4*	24	4	6	-	-	-	1	2	1	2	8-ch	TSSOP28
ML51UB9AE	16	1	4*	24	4	6	-	-	-	1	2	1	2	8-ch	SOP28
ML51PB9AE	16	1	4*	28	4	6	2	Y	2	1	2	2	2	8-ch	LQFP32
ML51TB9AE	16	1	4*	28	4	6	2	Y	2	1	2	2	2	8-ch	QFN33
ML51EC0AE	32	2	4*	24	4	6	2	Y	2	1	2	2	2	8-ch	TSSOP28
ML51UC0AE	32	2	4*	24	4	6	2	Y	2	1	2	2	2	8-ch	SOP28
ML51PC0AE	32	2	4*	28	4	6	2	Y	2	1	2	2	2	8-ch	LQFP32
ML51TC0AE	32	2	4*	28	4	6	2	Y	2	1	2	2	2	8-ch	QFN33

* ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.

** ISO-7816 also can define as standard UART function.

3.2 ML51 Series Selection Code



4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuaration informations by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 ML51 Series Pin Diagram

4.1.1.1 QFN33 Package

Corresponding Part Number: ML51TC0AE / ML51TB9AE

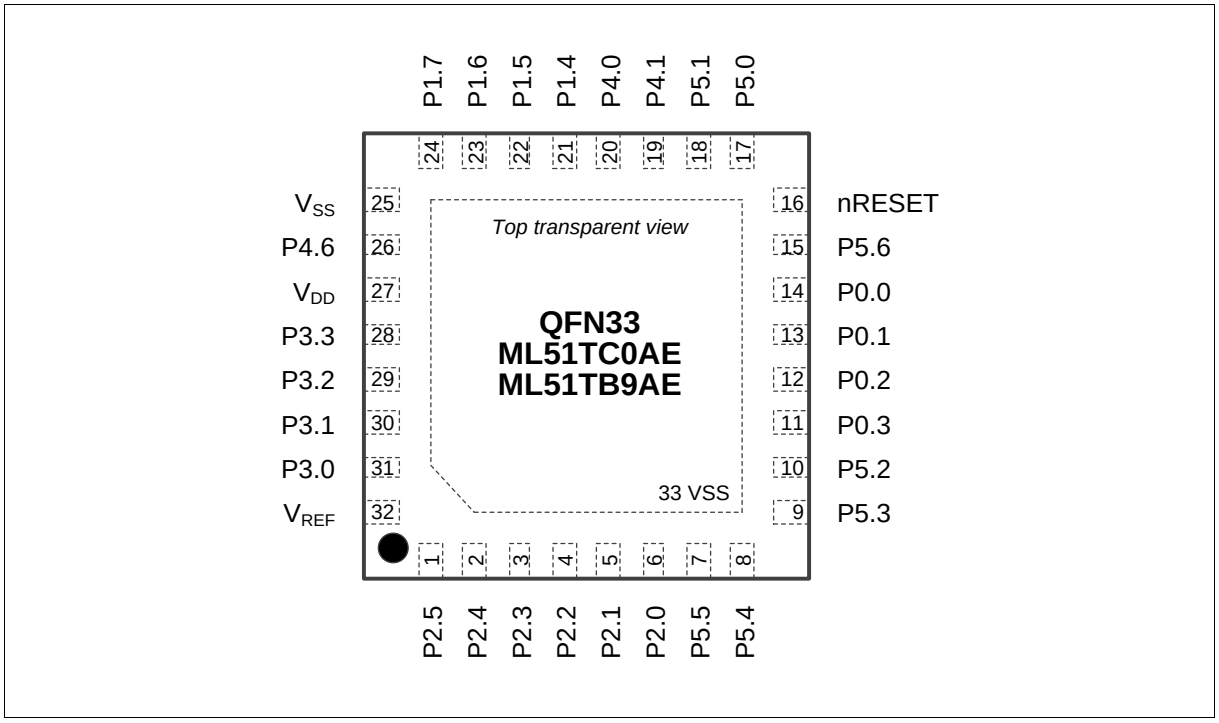


Figure 4.1-1 Pin Assignment of QFN-33 Package

4.1.1.2 LQFP32 Package

Corresponding Part Number: ML51PD1AE / ML51PC0AE / ML51PB9AE

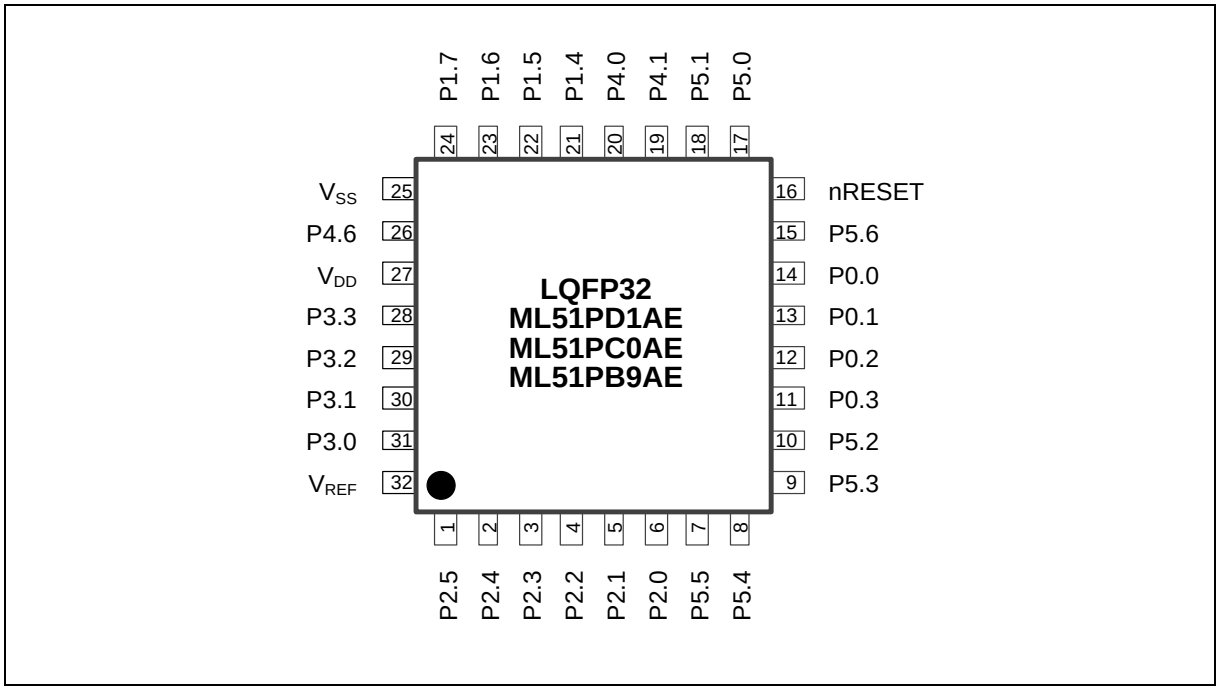


Figure 4.1-2 Pin Assignment of LQFP-32 Package

4.1.1.3 TSSOP28 Package

Corresponding Part Number: ML51EC0AE / ML51EB9AE

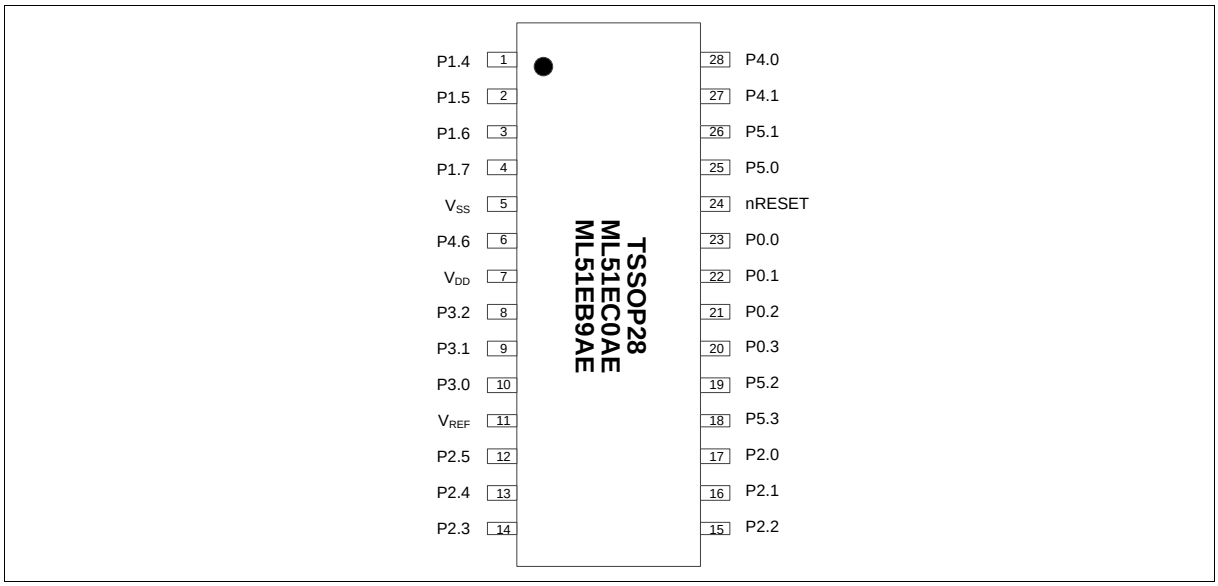


Figure 4.1-3 Pin Assignment of TSSOP-28 Package

4.1.1.4 SOP28 Package

Corresponding Part Number: ML51UC0AE / ML51UB9AE

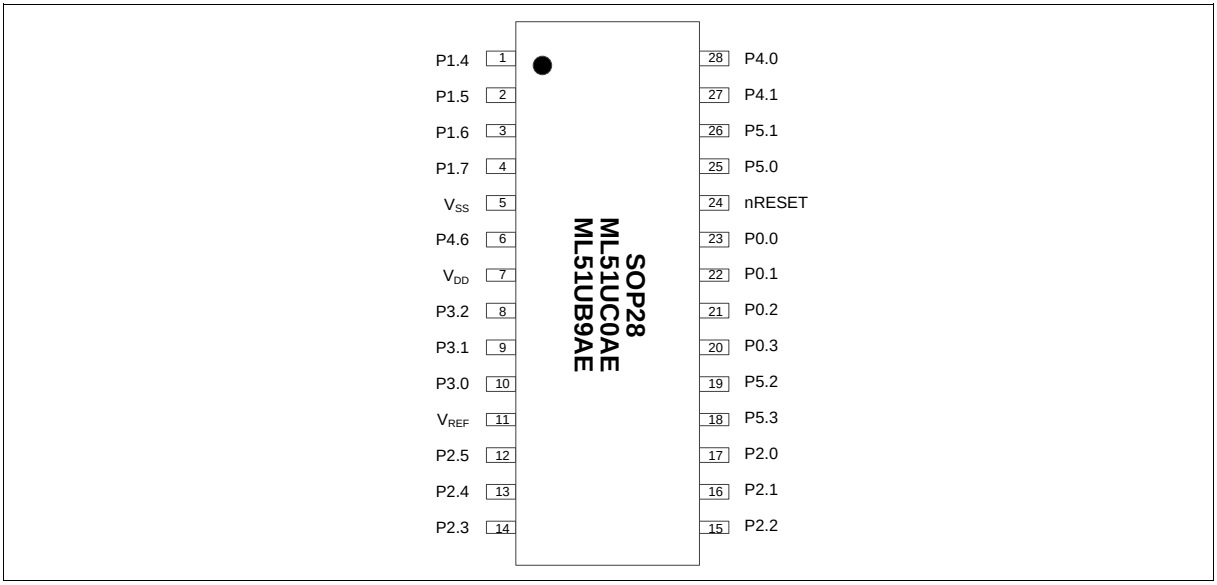


Figure 4.1-4 Pin Assignment of SOP-28 Package

4.1.1.5 TSSOP20 Package

Corresponding Part Number: ML51FB9AE

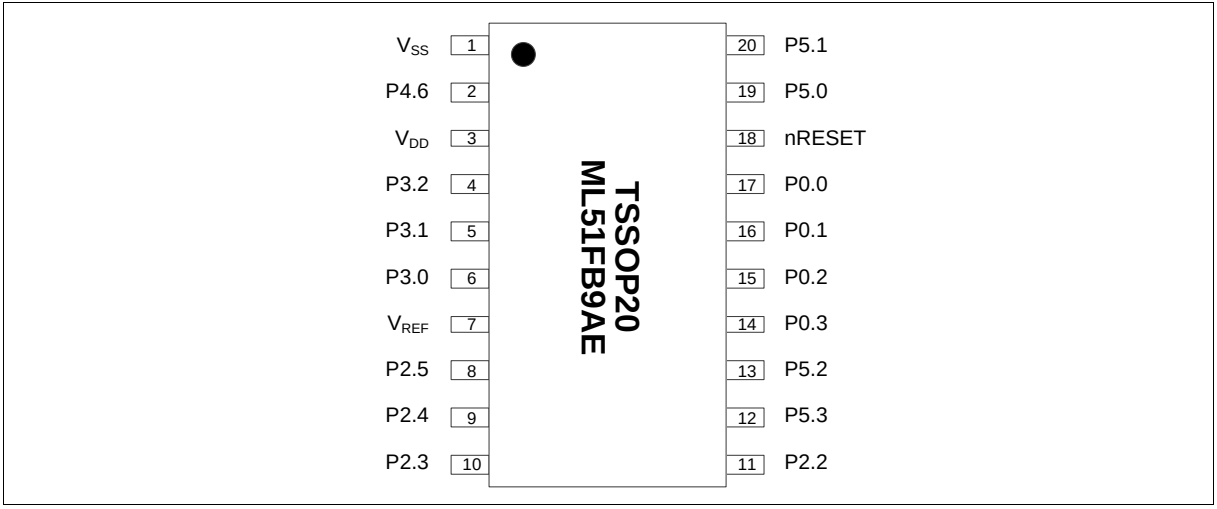


Figure 4.1-5 Pin Assignment of TSSOP-20 Package

4.1.1.6 SOP20 Package

Corresponding Part Number: ML51OB9AE

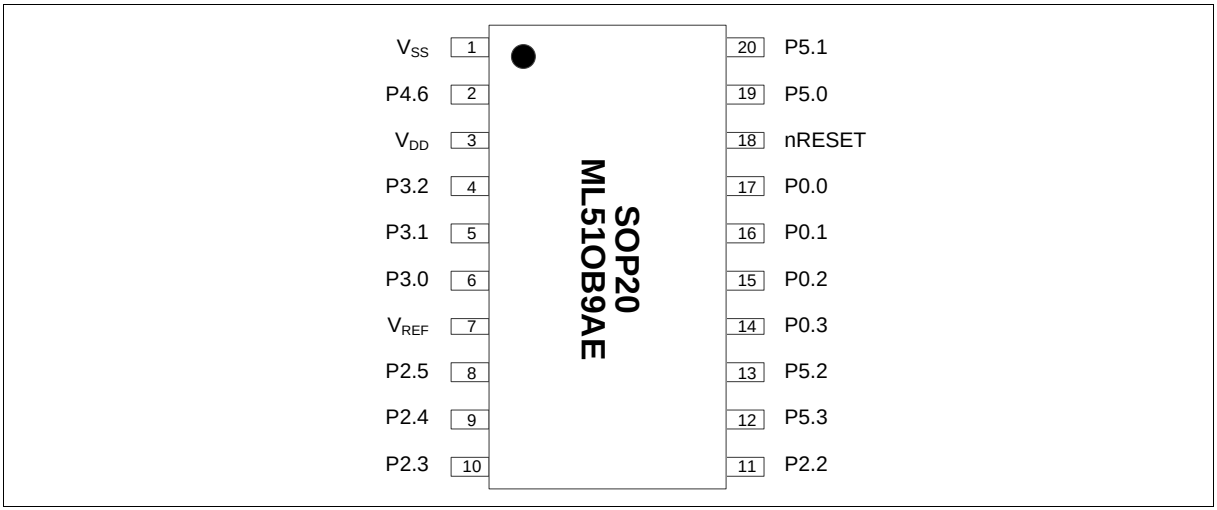


Figure 4.1-6 Pin Assignment of TSSOP-20 Package

4.1.1.7 QFN20 Package

Corresponding Part Number: ML51XB9AE

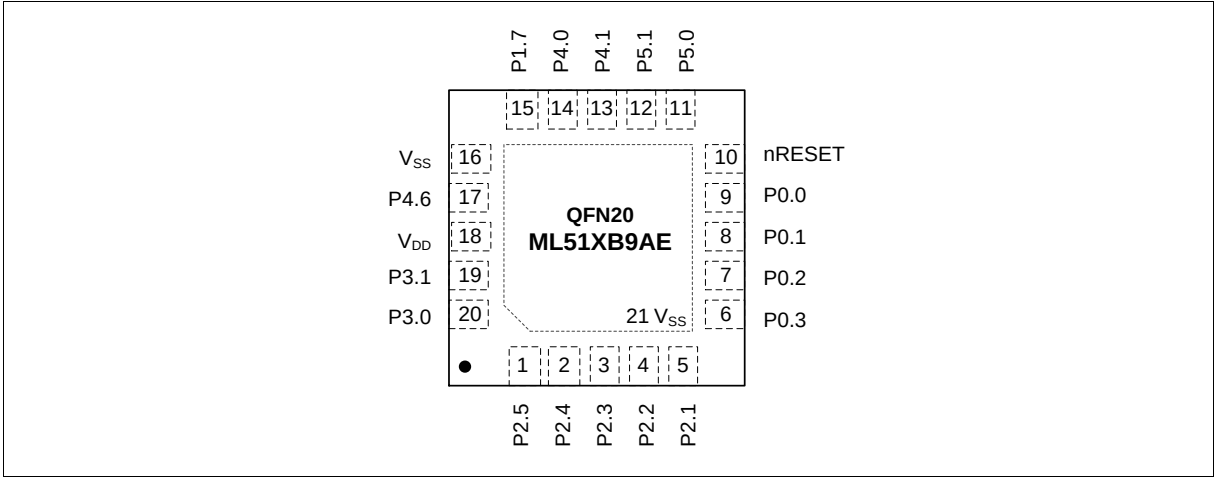


Figure 4.1-7 Pin Assignment of QFN-20 Package

4.1.1.8 TSSOP14 Package

Corresponding Part Number: ML51DB9AE

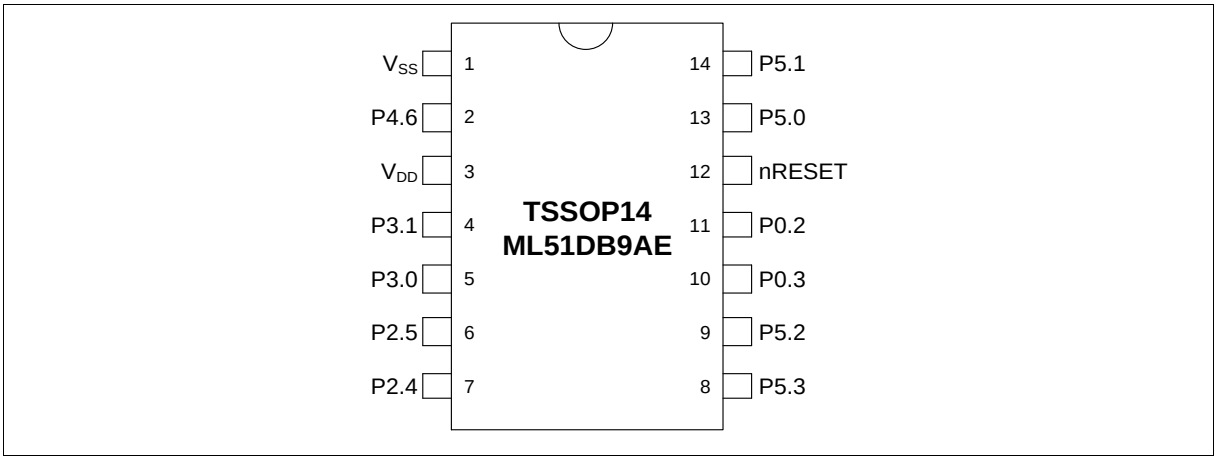


Figure 4.1-8 Pin Assignment of TSSOP-14 Package

4.1.1.9 MSOP10 Package

Corresponding Part Number: ML51BB9AE

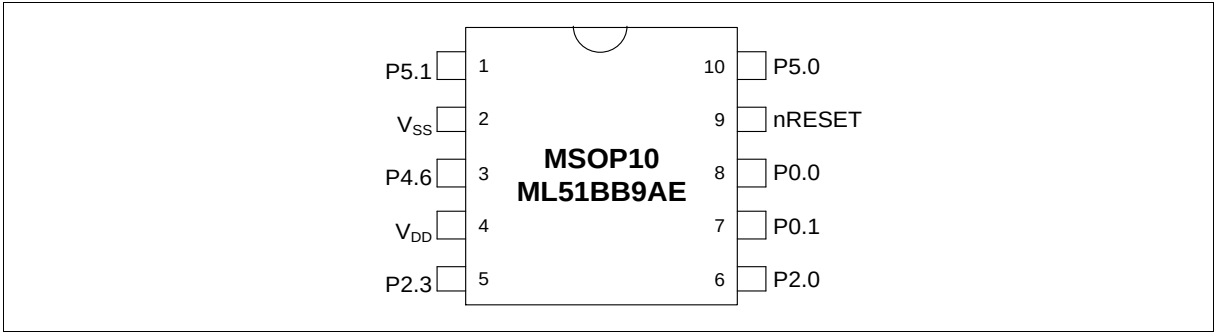


Figure 4.1-9 Pin Assignment of MSOP-10 Package

4.1.2 ML51 Series Multi Function Pin Diagram

4.1.2.1 QFN33 Package

Corresponding Part Number: ML51TC0AE / ML51TB9AE

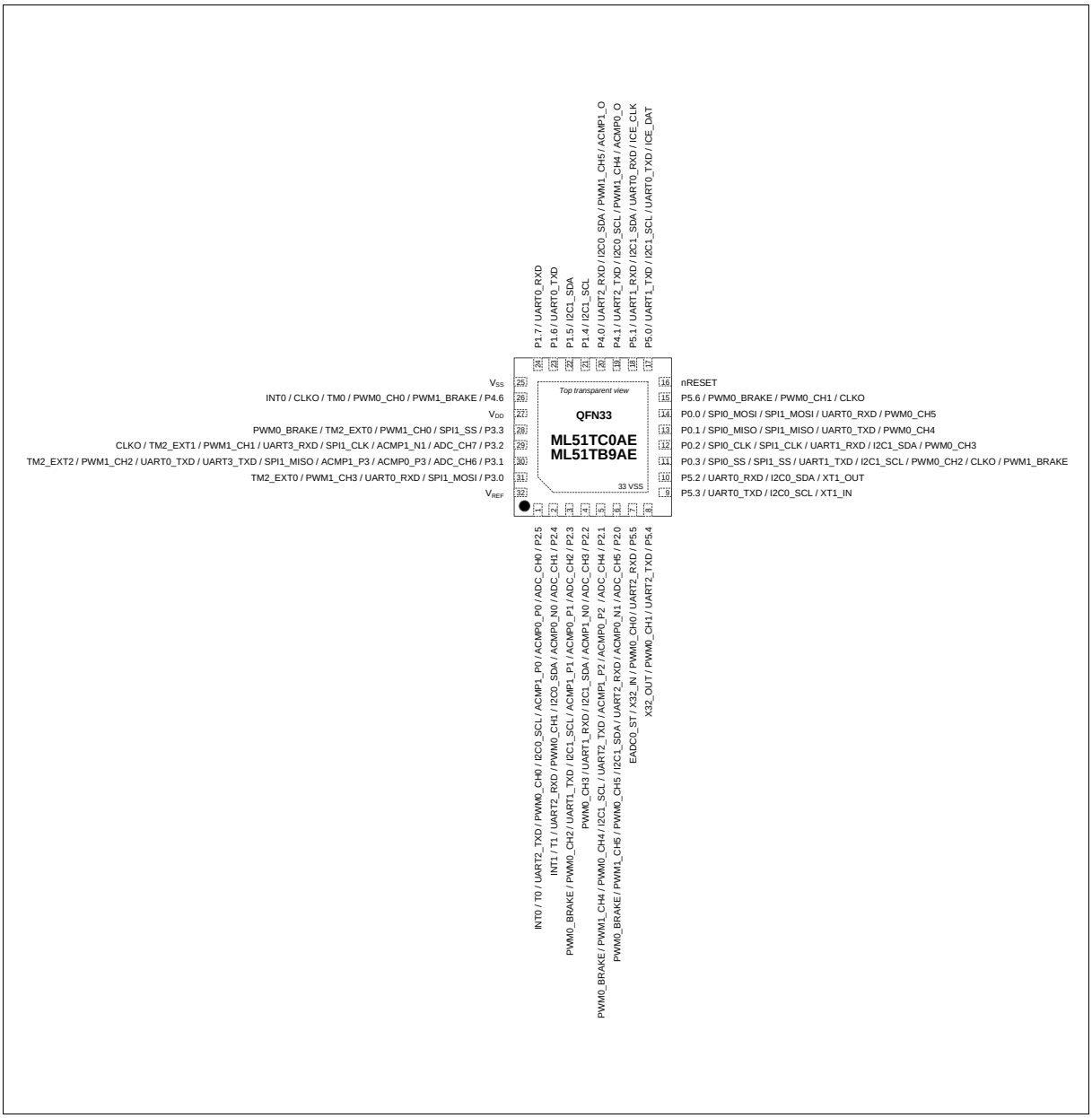


Figure 4.1-10 Multi Function Pin Assignment of QFN-33 Package

4.1.2.2 LQFP32 Package

Corresponding Part Number: ML51PD1AE / ML51PC0AE / ML51PB9AE

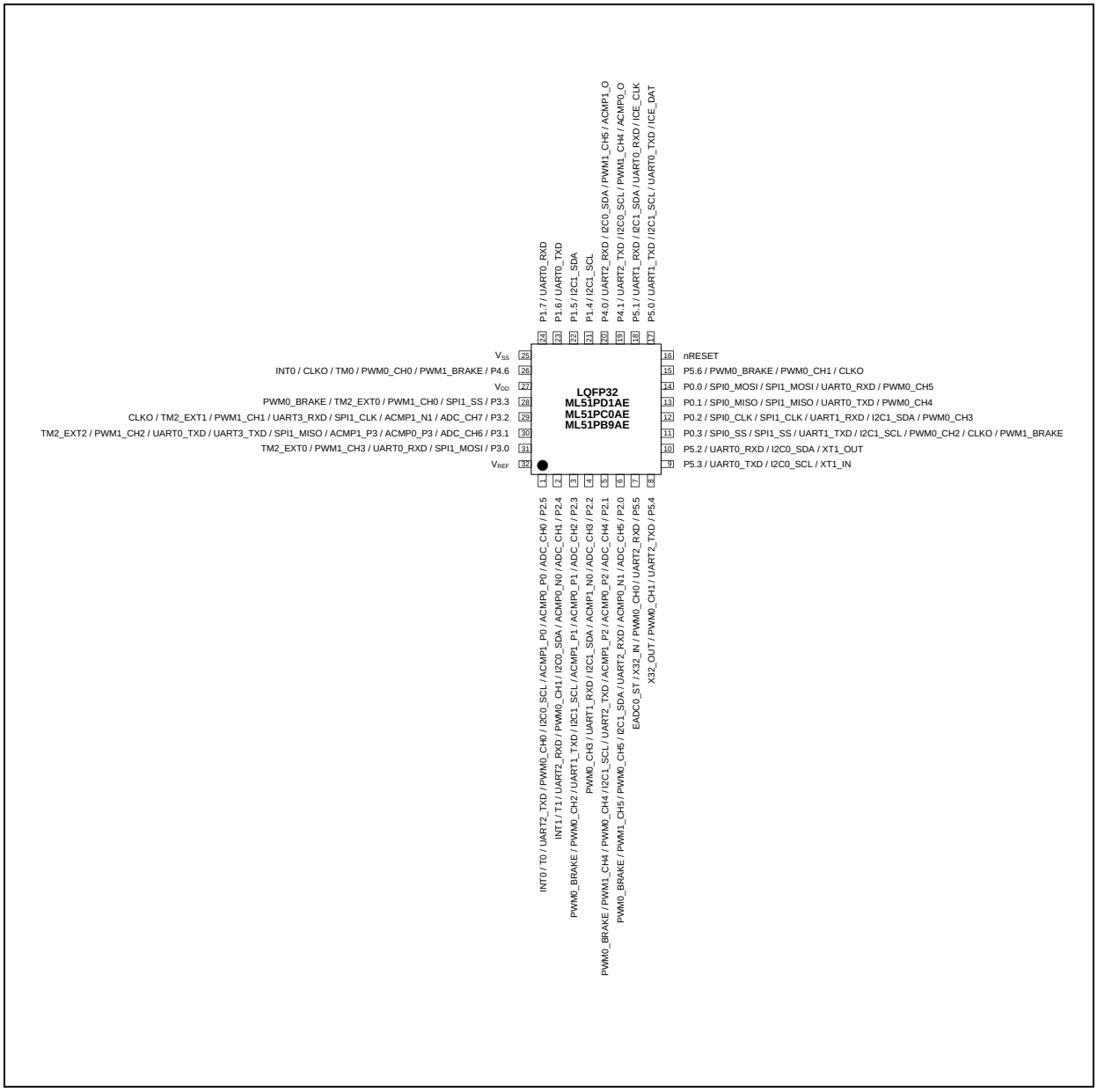


Figure 4.1-11 Multi Function Pin Assignment of LQFP-32 Package

4.1.2.3 TSSOP28 Package

Corresponding Part Number:ML51EC0AE / ML51EB9AE

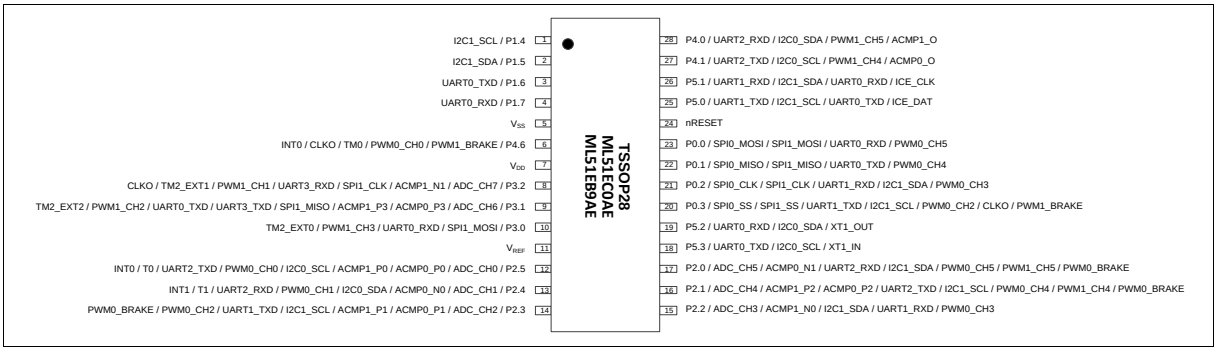


Figure 4.1-12 Multi Function Pin Assignment of TSSOP-28 Package

4.1.2.4 SOP28 Package

Corresponding Part Number:ML51UC0AE / ML51UB9AE

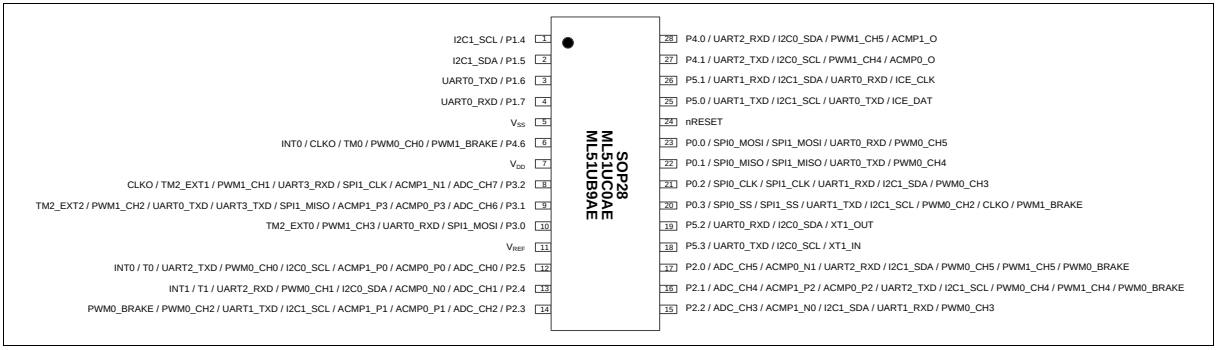


Figure 4.1-13 Multi Function Pin Assignment of SOP-28 Package

4.1.2.5 TSSOP20 Package

Corresponding Part Number: ML51FB9AE

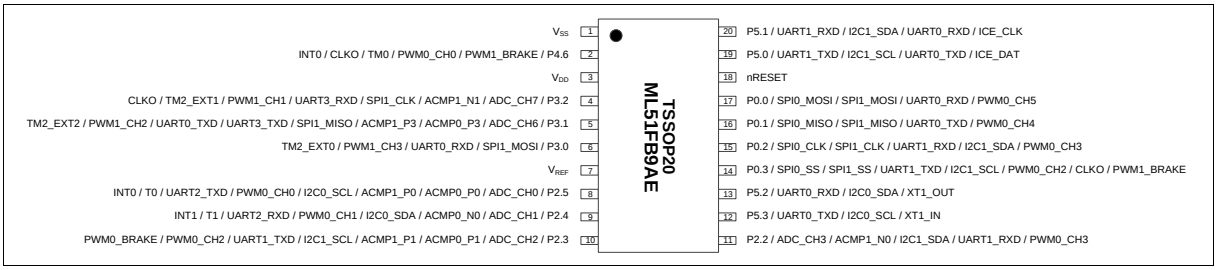


Figure 4.1-14 Multi Function Pin Assignment of TSSOP-20 Package

4.1.2.6 SOP20 Package

Corresponding Part Number: ML51OB9AE

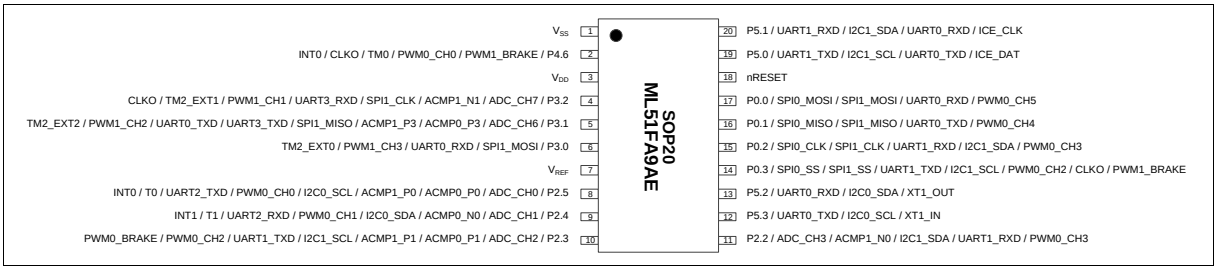


Figure 4.1-15 Multi Function Pin Assignment of SOP-20 Package

4.1.2.7 QFN20 Package

Corresponding Part Number:ML51XB9AE

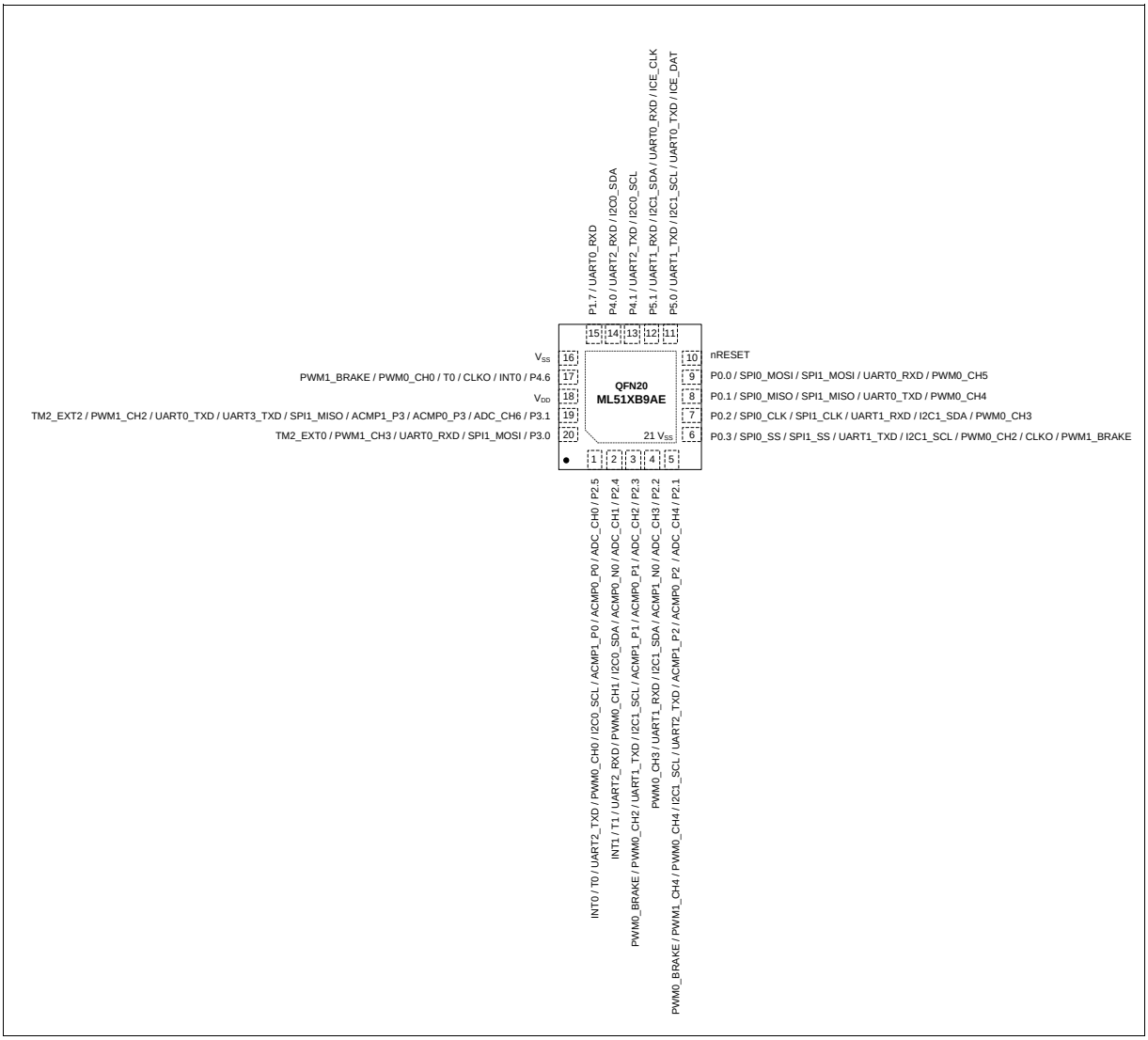


Figure 4.1-16 Multi Function Pin Assignment of QFN-20 Package

4.1.2.8 TSSOP14 Package

Corresponding Part Number: ML51DB9AE

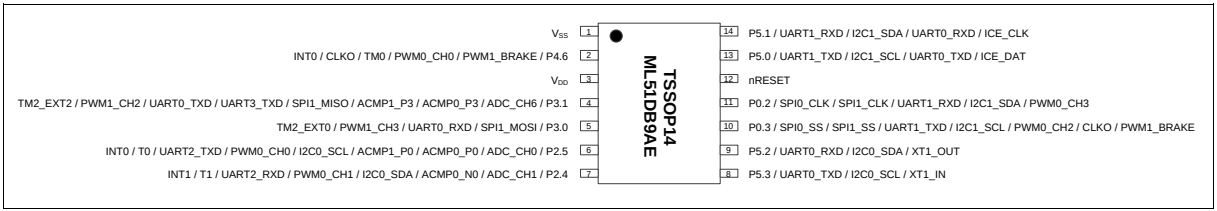


Figure 4.1-17 Multi Function Pin Assignment of Package

4.1.2.9 MSOP10 Package

Corresponding Part Number: ML51BB9AE

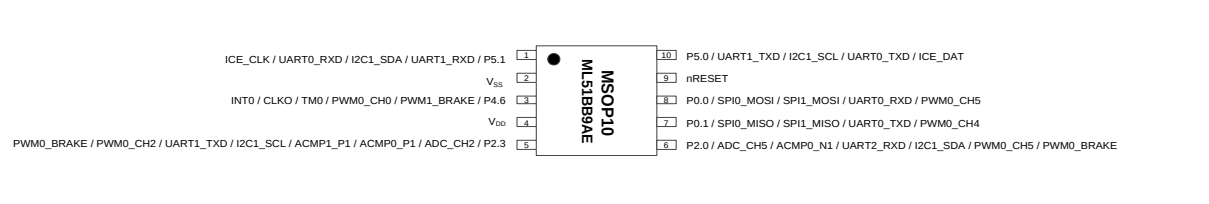


Figure 4.1-18 Pin Assignment of MSOP-10 Package

4.2 Pin Description

The default multi-function pin (MFPx = 0x00) is the GPIO pin. After setting MFPx as non-zero value, the GPIO pin will ANDed with a select function. A simple multi-function demo code for UART0 is given below:

```
SFRS = 0x02;              ;switch to SFR page 2
P3MF10 = 0x56;            ;set P30 as UART0_RXD and P31 as UART0_TXD
```

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
-	6	1	8	12	1	1	P2.5	MFP0	General purpose digital I/O pin.	
							ADC_CH0	MFP1	GPIO	ADC channel 0 analog input.
							ACMP0_P0	MFP1	GPIO	Analog comparator 0 positive input 0 pin.
							ACMP1_P0	MFP1	GPIO	Analog comparator 1 positive input 0 pin.
							I^2C0_SCL	MFP6	GPIO	I^2C0 clock pin.
							PWM0_CH0	MFP11	GPIO	PWM0 channel 0 output.
							UART2_TXD	MFP13	GPIO	UART2 data transmitter output pin.
							SC0_CLK	MFP13	GPIO	Smart Card 0 clock pin.
							T0	MFP14	GPIO	Timer0 counter input/toggle output pin.
							INT0	MFP15	GPIO	External interrupt 0 input pin.
-	7	2	9	13	2	2	P2.4	MFP0	General purpose digital I/O pin.	
							ADC_CH1	MFP1	GPIO	ADC channel 1 analog input.
							ACMP0_N0	MFP1	GPIO	Analog comparator 0 negative input 0 pin.
							I^2C0_SDA	MFP6	GPIO	I^2C0 data input/output pin.
							PWM0_CH1	MFP11	GPIO	PWM0 channel 1 output.
							UART2_RXD	MFP13	GPIO	UART2 data receiver input pin.
							SC0_DAT	MFP13	GPIO	Smart Card 0 data pin.
							T1	MFP14	GPIO	Timer1 event counter input/toggle output pin.
							INT1	MFP15	GPIO	External interrupt 1 input pin.
5	-	3	10	14	3	3	P2.3	MFP0	General purpose digital I/O pin.	
							ADC_CH2	MFP1	GPIO	ADC channel 2 analog input.
							ACMP0_P1	MFP1	GPIO	Analog comparator 0 positive input 1 pin.
							ACMP1_P1	MFP1	GPIO	Analog comparator 1 positive input 1 pin.
							I^2C1_SCL	MFP4	GPIO	I^2C1 clock pin.
							UART1_TXD	MFP6	GPIO	UART1 data transmitter output pin.

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
							PWM0_CH2	MFP11	GPIO	PWM0 channel 2 output.
							PWM0_BRAKE	MFP13	GPIO	PWM0 Brake input pin.
-	-	4	11	15	4	4	P2.2	MFP0	General purpose digital I/O pin.	
							ADC_CH3	MFP1	GPIO	ADC channel 3 analog input.
							ACMP1_N0	MFP1	GPIO	Analog comparator 1 negative input 0 pin.
							I^2C1_SDA	MFP4	GPIO	I^2C1 data input/output pin.
							UART1_RXD	MFP6	GPIO	UART1 data receiver input pin.
							PWM0_CH3	MFP11	GPIO	PWM0 channel 3 output.
-	-	5	-	16	5	5	P2.1	MFP0	General purpose digital I/O pin.	
							ADC_CH4	MFP1	GPIO	ADC channel 4 analog input.
							ACMP0_P2	MFP1	GPIO	Analog comparator 0 positive input 2 pin.
							ACMP1_P2	MFP1	GPIO	Analog comparator 1 positive input 2 pin.
							UART2_TXD	MFP7	GPIO	UART2 data transmitter output pin.
							SC0_CLK	MFP7	GPIO	Smart Card 0 clock pin.
							I^2C1_SCL	MFP9	GPIO	I^2C1 clock pin.
							PWM0_CH4	MFP11	GPIO	PWM0 channel 4 output.
							PWM1_CH4	MFP12	GPIO	PWM1 channel 4 output.
							PWM0_BRAKE	MFP13	GPIO	PWM0 Brake input pin.
6	-	-	-	17	6	6	P2.0	MFP0	General purpose digital I/O pin.	
							ADC_CH5	MFP1	GPIO	ADC channel 5 analog input.
							ACMP0_N1	MFP1	GPIO	Analog comparator 0 negative input 1 pin.
							UART2_RXD	MFP7	GPIO	UART2 data receiver input pin.
							SC0_DAT	MFP7	GPIO	Smart Card 0 data pin.
							I^2C1_SDA	MFP9	GPIO	I^2C1 data input/output pin.
							PWM0_CH5	MFP11	GPIO	PWM0 channel 5 output.
							PWM1_CH5	MFP12	GPIO	PWM1 channel 5 output.
							PWM1_BRAKE	MFP13	GPIO	PWM1 Brake input pin.
-	-	-	-	-	-	7	P1.3	MFP0	General purpose digital I/O pin.	
							IC0	MFP13	GPIO	Input Capture channel 0
-	-	-	-	-	-	8	P1.2	MFP0	General purpose digital I/O pin.	
							UART3_TXD	MFP6	GPIO	UART3 data transmitter output pin.
							SC1_CLK	MFP6	GPIO	Smart Card 1 clock pin.

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
							IC1	MFP13	GPIO	Input Capture channel 1
-	-	-	-	-	-	9	P1.1	MFP0	General purpose digital I/O pin.	
							UART3_RXD	MFP6	GPIO	UART3 data receiver input pin.
							SC1_DAT	MFP6	GPIO	Smart Card 1 data pin.
							UART1_TXD	MFP7	GPIO	UART1 data transmitter output pin.
							IC2	MFP13	GPIO	Input Capture channel 2
-	-	-	-	-	-	10	P1.0	MFP0	General purpose digital I/O pin.	
							IC0	MFP13	GPIO	Input Capture channel 0
-	-	-	-	-	7	11	P5.5	MFP0	General purpose digital I/O pin.	
							UART2_RXD	MFP2	GPIO	UART2 data receiver input pin.
							SC0_DAT	MFP2	GPIO	Smart Card 0 data pin.
							PWM0_CH0	MFP7	GPIO	PWM0 channel 0 output.
							X32_IN	MFP10	External 32.768 kHz crystal input pin.	
							STADC	MFP11	GPIO	ADC external trigger input.
-	-	-	-	-	8	12	P5.4	MFP0	General purpose digital I/O pin.	
							UART2_TXD	MFP2	GPIO	UART2 data transmitter output pin.
							SC0_CLK	MFP2	GPIO	Smart Card 0 clock pin.
							PWM0_CH1	MFP7	GPIO	PWM0 channel 1 output.
							X32_OUT	MFP10	External 32.768 kHz crystal output pin.	
-	8	-	12	18	9	13	P5.3	MFP0	General purpose digital I/O pin.	
							UART0_TXD	MFP3	GPIO	UART0 data transmitter output pin.
							I^2C0_SCL	MFP4	GPIO	I^2C0 clock pin.
							XT1_IN	MFP10	External 4~24 MHz (high speed) crystal input pin.	
-	9	-	13	19	10	14	P5.2	MFP0	General purpose digital I/O pin.	
							UART0_RXD	MFP3	GPIO	UART0 data receiver input pin.
							I^2C0_SDA	MFP4	GPIO	I^2C0 data input/output pin.
							XT1_OUT	MFP10	External 4~24 MHz (high speed) crystal output pin.	
-	-	-	-	-	-	15	P0.7	MFP0	General purpose digital I/O pin.	
							UART0_TXD	MFP7	GPIO	UART0 data transmitter output pin.
							I^2C1_SCL	MFP8	GPIO	I^2C1 clock pin.
							PWM1_CH4	MFP11	GPIO	PWM1 channel 4 output.
							INT1	MFP15	GPIO	External interrupt 1 input pin.

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
-	-	-	-	-	-	16	P0.6	MFP0	General purpose digital I/O pin.	
							UART0_RXD	MFP7	GPIO	UART0 data receiver input pin.
							I²C1_SDA	MFP8	GPIO	I²C1 data input/output pin.
							PWM1_CH5	MFP11	GPIO	PWM1 channel 5 output.
							INT0	MFP15	GPIO	External interrupt 0 input pin.
-	-	-	-	-	-	17	P0.5	MFP0	General purpose digital I/O pin.	
							UART0_TXD	MFP8	GPIO	UART0 data transmitter output pin.
							I²C0_SCL	MFP9	GPIO	I²C0 clock pin.
							PWM0_CH0	MFP13	GPIO	PWM0 channel 0 output.
-	-	-	-	-	-	18	P0.4	MFP0	General purpose digital I/O pin.	
							UART0_RXD	MFP8	GPIO	UART0 data receiver input pin.
							I²C0_SDA	MFP9	GPIO	I²C0 data input/output pin.
							PWM0_CH1	MFP13	GPIO	PWM0 channel 1 output.
-	10	6	14	20	11	19	P0.3	MFP0	General purpose digital I/O pin.	
							SPI0_SS	MFP3	GPIO	SPI0 slave select pin.
							SPI1_SS	MFP4	GPIO	SPI1 slave select pin.
							UART1_TXD	MFP8	GPIO	UART1 data transmitter output pin.
							I²C1_SCL	MFP9	GPIO	I²C1 clock pin.
							STADC	MFP11	GPIO	ADC external trigger input.
							PWM0_CH2	MFP13	GPIO	PWM0 channel 2 output.
							PWM1_BRAKE	MFP15	GPIO	PWM1 Brake input pin.
-	11	7	15	21	12	20	P0.2	MFP0	General purpose digital I/O pin.	
							SPI0_CLK	MFP3	GPIO	SPI0 serial clock pin.
							SPI1_CLK	MFP4	GPIO	SPI1 serial clock pin.
							UART1_RXD	MFP8	GPIO	UART1 data receiver input pin.
							I²C1_SDA	MFP9	GPIO	I²C1 data input/output pin.
							PWM0_CH3	MFP13	GPIO	PWM0 channel 3 output.
7	-	8	16	22	13	21	P0.1	MFP0	General purpose digital I/O pin.	
							SPI0_MISO	MFP3	GPIO	SPI0 MISO (Master In, Slave Out) pin.
							SPI1_MISO	MFP4	GPIO	SPI1 MISO (Master In, Slave Out) pin.
							UART0_TXD	MFP7	GPIO	UART0 data transmitter output pin.
							PWM0_CH4	MFP13	GPIO	PWM0 channel 4 output.

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
8	-	9	17	23	14	22	P0.0	MFP0	General purpose digital I/O pin.	
							SPI0_MOSI	MFP3	GPIO	SPI0 MOSI (Master Out, Slave In) pin.
							SPI1_MOSI	MFP4	GPIO	SPI1 MOSI (Master Out, Slave In) pin.
							UART0_RXD	MFP7	GPIO	UART0 data receiver input pin.
							PWM0_CH5	MFP13	GPIO	PWM0 channel 5 output.
-	-	-	-	-	15	23	P5.6	MFP0	General purpose digital I/O pin.	
							PWM0_BRAKE	MFP11	GPIO	PWM0 Brake input pin.
							PWM0_CH1	MFP12	GPIO	PWM0 channel 1 output.
							CLKO	MFP14	GPIO	Clock Out
9	12	10	18	24	16	24	$\overline{\text{RST}}$		External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.	
10	13	11	19	25	17	25	P5.0	MFP0	General purpose digital I/O pin.	
							UART1_TXD	MFP2	GPIO	UART1 data transmitter output pin.
							I^2C1_SCL	MFP3	GPIO	I^2C1 clock pin.
							UART0_TXD	MFP4	GPIO	UART0 data transmitter output pin.
							ICE_DAT	MFP14	GPIO	Serial wired debugger data pin.
1	14	12	20	26	18	26	P5.1	MFP0	General purpose digital I/O pin.	
							UART1_RXD	MFP2	GPIO	UART1 data receiver input pin.
							I^2C1_SDA	MFP3	GPIO	I^2C1 data input/output pin.
							ICE_CLK	MFP14	GPIO	Serial wired debugger clock pin.
-	-	-	-	-	-	27	P4.5	MFP0	General purpose digital I/O pin.	
							UART2_TXD	MFP8	GPIO	UART2 data transmitter output pin.
							SC0_CLK	MFP8	GPIO	Smart Card 0 clock pin.
							I^2C1_SCL	MFP9	GPIO	I^2C1 clock pin.
							PWM1_CH0	MFP12	GPIO	PWM1 channel 0 output.
-	-	-	-	-	-	28	P4.4	MFP0	General purpose digital I/O pin.	
							UART2_RXD	MFP8	GPIO	UART2 data receiver input pin.
							SC0_DAT	MFP8	GPIO	Smart Card 0 data pin.
							I^2C1_SDA	MFP9	GPIO	I^2C1 data input/output pin.
							PWM1_CH1	MFP12	GPIO	PWM1 channel 1 output.
-	-	-	-	-	-	29	P4.3	MFP0	General purpose digital I/O pin.	
							PWM1_CH2	MFP12	GPIO	PWM1 channel 2 output.
-	-	-	-	-	-	30	P4.2	MFP0	General purpose digital I/O pin.	

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
							PWM1_CH3	MFP12	GPIO	PWM1 channel 3 output.
-	-	13	-	27	19	31	P4.1	MFP0	General purpose digital I/O pin.	
							UART2_TXD	MFP8	GPIO	UART2 data transmitter output pin.
							SC0_CLK	MFP8	GPIO	Smart Card 0 clock pin.
							I^2C0_SCL	MFP9	GPIO	I^2C0 clock pin.
							PWM1_CH4	MFP12	GPIO	PWM1 channel 4 output.
							ACMP0_O	MFP14	GPIO	Analog comparator 0 output pin.
-	-	14	-	28	20	32	P4.0	MFP0	General purpose digital I/O pin.	
							UART2_RXD	MFP8	GPIO	UART2 data receiver input pin.
							SC0_DAT	MFP8	GPIO	Smart Card 0 data pin.
							I^2C0_SDA	MFP9	GPIO	I^2C0 data input/output pin.
							PWM1_CH5	MFP12	GPIO	PWM1 channel 5 output.
							ACMP1_O	MFP14	GPIO	Analog comparator 1 output pin.
							INT1	MFP15	GPIO	External interrupt 1 input pin.
-	-	-	-	1	21	33	P1.4	MFP0	General purpose digital I/O pin.	
							I^2C1_SCL	MFP4	GPIO	I^2C1 clock pin.
-	-	-	-	2	22	34	P1.5	MFP0	General purpose digital I/O pin.	
							I^2C1_SDA	MFP4	GPIO	I^2C1 data input/output pin.
-	-	-	-	3	23	35	P1.6	MFP0	General purpose digital I/O pin.	
							UART0_TXD	MFP3	GPIO	UART0 data transmitter output pin.
-	-	15	-	4	24	36	P1.7	MFP0	General purpose digital I/O pin.	
							UART0_RXD	MFP3	GPIO	UART0 data receiver input pin.
							SC2_CLK	MFP7	GPIO	Smart Card 2 clock pin.
2	1	16	1	5	25	37	VSS		Ground pin for digital circuit.	
3	2	17	2	6	26	38	P4.6	MFP0	General purpose digital I/O pin.	
							PWM1_BRAKE	MFP11	GPIO	PWM1 Brake input pin.
							PWM0_CH0	MFP12	GPIO	PWM0 channel 0 output.
							T0	MFP13	GPIO	Timer0 counter input/toggle output pin.
							CLKO	MFP14	GPIO	Clock Out
							INT0	MFP15	GPIO	External interrupt 0 input pin.
4	3	18	3	7	27	39	V_{DD}		Power supply for I/O ports	
-	-	-	-	-	-	40	P4.7	MFP0	General purpose digital I/O pin.	

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
							T1	MFP13	GPIO	Timer1 event counter input/toggle output pin.
-	-	-	-	-	28	41	P3.3	MFP0	General purpose digital I/O pin.	
							SPI1_SS	MFP4	GPIO	SPI1 slave select pin.
							PWM1_CH0	MFP11	GPIO	PWM1 channel 0 output.
							IC0	MFP13	GPIO	Input Capture channel 0
							PWM0_BRAKE	MFP15	GPIO	PWM0 Brake input pin.
-	-	-	4	8	29	42	P3.2	MFP0	General purpose digital I/O pin.	
							ADC_CH7	MFP1	GPIO	ADC channel 7 analog input.
							ACMP1_N1	MFP1	GPIO	Analog comparator 1 negative input 1 pin.
							SPI1_CLK	MFP4	GPIO	SPI1 serial clock pin.
							UART3_RXD	MFP7	GPIO	UART3 data receiver input pin.
							SC1_DAT	MFP7	GPIO	Smart Card 1 data pin.
							PWM1_CH1	MFP11	GPIO	PWM1 channel 1 output.
							IC1	MFP13	GPIO	Input Capture channel 1
							CLKO	MFP14	GPIO	Clock Out
-	4	19	5	9	30	43	P3.1	MFP0	General purpose digital I/O pin.	
							ADC_CH6	MFP1	GPIO	ADC channel 6 analog input.
							ACMP0_P3	MFP1	GPIO	Analog comparator 0 positive input 3 pin.
							ACMP1_P3	MFP1	GPIO	Analog comparator 1 positive input 3 pin.
							SPI1_MISO	MFP4	GPIO	SPI1 MISO (Master In, Slave Out) pin.
							UART3_TXD	MFP5	GPIO	UART3 data transmitter input pin.
							SC1_DAT	MFP5	GPIO	Smart Card 1 clock pin.
							UART0_TXD	MFP6	GPIO	UART0 data transmitter output pin.
							PWM1_CH2	MFP11	GPIO	PWM1 channel 2 output.
							IC2	MFP13	GPIO	Input Capture channel 2
-	5	20	6	10	31	44	P3.0	MFP0	General purpose digital I/O pin.	
							SPI1_MOSI	MFP4	GPIO	SPI1 MOSI (Master Out, Slave In) pin.
							UART0_RXD	MFP6	GPIO	UART0 data receiver input pin.
							PWM1_CH3	MFP11	GPIO	PWM1 channel 3 output/capture input.
							IC0	MFP13	GPIO	Input Capture channel 0
4	3	18	7	11	32	45	V_{REF}		ADC reference voltage input. **Note:** This pin needs to be connected with a 0.1uF capacitor.	
2	1	16	1	5	25	46	AVSS		Ground pin for analog circuit.	

MSOP10	TSSOP14	QFN20	TSSOP20	TSSOP28	QFN33	LQFP48	Pin Name	MFP[1]	Description[2] [3] [4]	
-	-	-	-	-	-	47	P2.7	MFP0	General purpose digital I/O pin.	
							UART1_TXD	MFP6	GPIO	UART1 data transmitter output pin.
							PWM1_BRAKE	MFP11	GPIO	PWM1 Brake input pin.
							PWM1_CH4	MFP12	GPIO	PWM1 channel 4 output/capture input.
							ACMP0_O	MFP15	GPIO	Analog comparator 0 output pin.
-	-	-	-	-	-	48	P2.6	MFP0	General purpose digital I/O pin	
							UART1_RXD	MFP6	GPIO	UART1 data receiver input pin.
							PWM1_BRAKE	MFP11	GPIO	PWM1 Brake input pin.
							PWM1_CH5	MFP12	GPIO	PWM1 channel 5 output/capture input.
							ACMP1_O	MFP15	GPIO	Analog comparator 1 output pin.

[1] MFP* = Multi-function pin.
P0.0 MFP0 means P0MF10[3:0] = 0x0.
P0.1 MFP5 means P0MF10[7:4] = 0x5.

[2] Pin output mode be decided by PxMx, except for ACMP output, F_{SYS} clock output, SPI and Smart Card.
[3] All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description.
[4] GPIO = General purpose digital I/O pin.

5 BLOCK DIAGRAM

Figure 4.2-1 shows the ML51 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

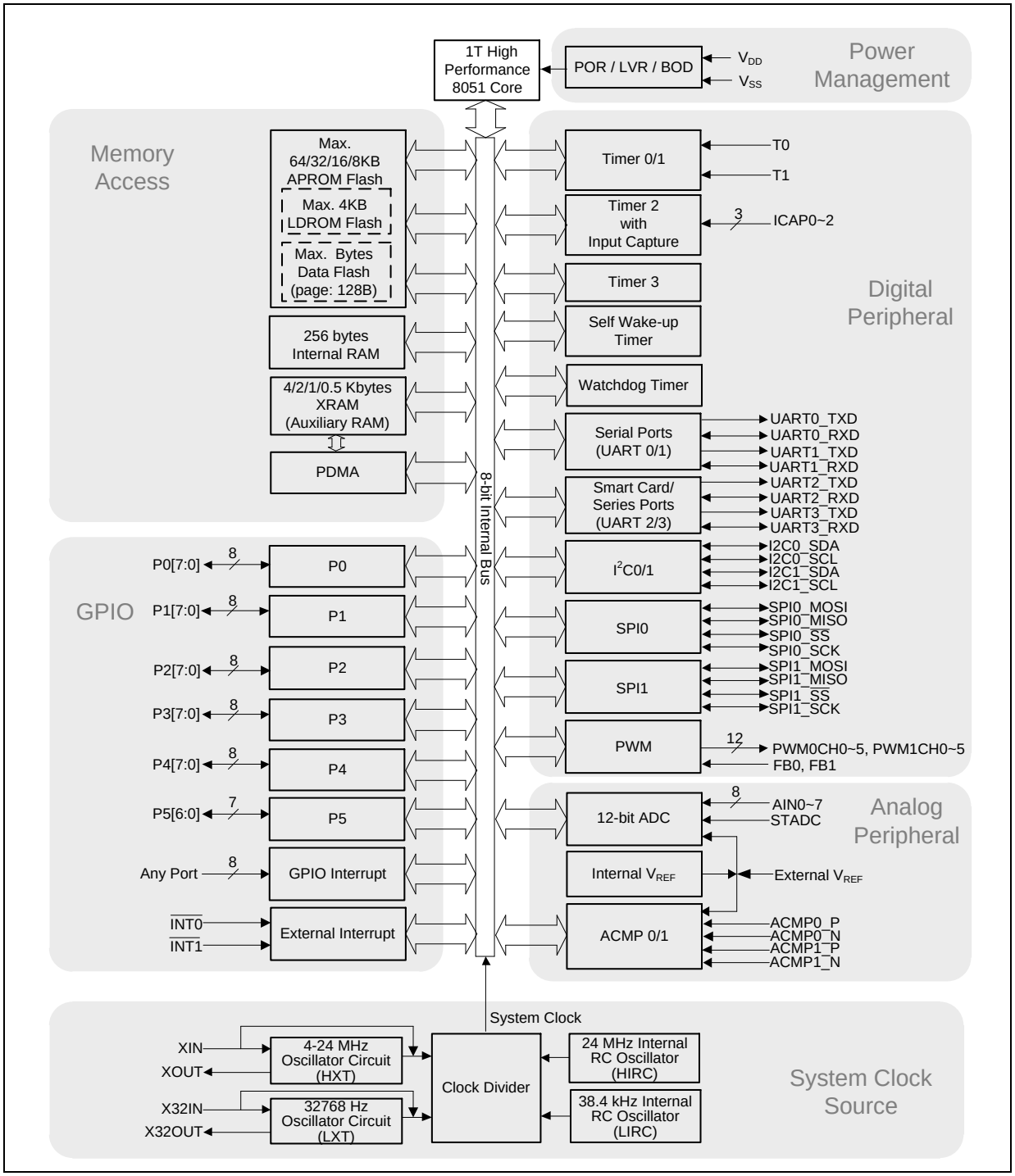


Figure 4.2-1 Functional Block Diagram

6 APPLICATION CIRCUIT

6.1 Power supply scheme

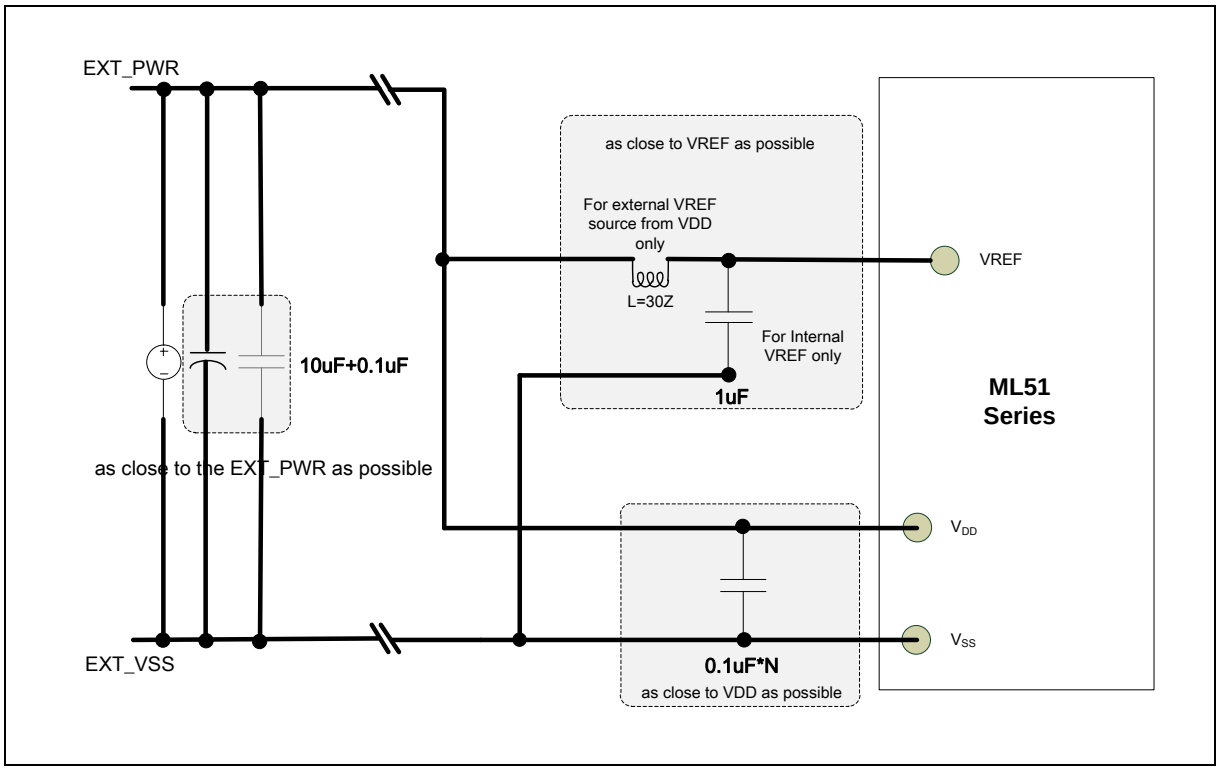


Figure 6.1 NuMicro® ML51 Power supply circuit

6.2 Peripheral Application scheme

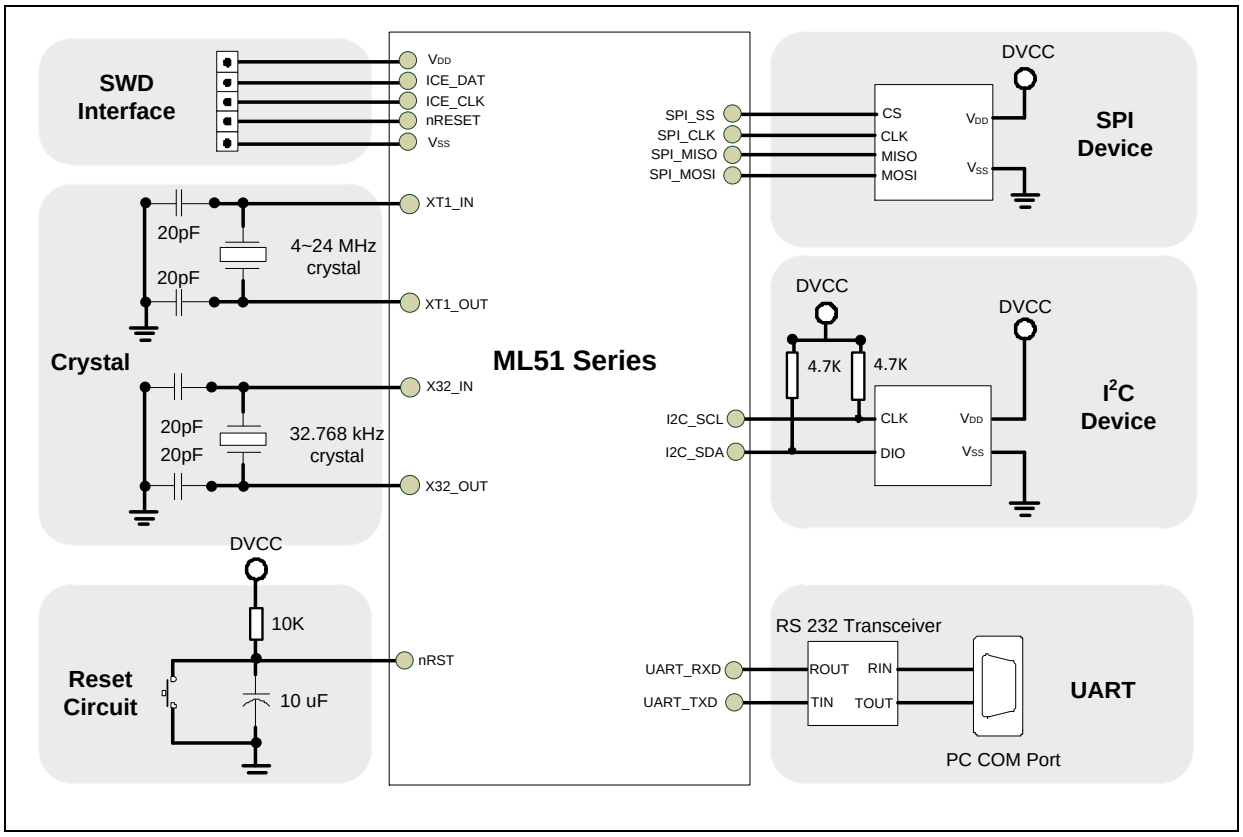


Figure 6.2 NuMicro® ML51 Peripheral interface circuit

6.3 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from several register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset (WDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])

6.3.1 Hardware Reset Sources

6.3.1.1 Power-On Reset and Low Voltage Reset

The ML51 incorporates an internal power-on reset (POR) and a low voltage reset (LVR). During a power-on process of rising power supply voltage V_{DD}, the POR or LVR will hold the MCU in reset mode when V_{DD} is lower than the voltage reference thresholds. This design makes CPU not access program flash while the V_{DD} is not adequate performing the flash reading. If an undetermined operating code is read from the program flash and executed, this will put CPU and even the whole system in to an erroneous state. After a while, V_{DD} rises above the threshold where the system can work, the selected oscillator will start and then program code will execute from 0000H. At the same time, a power-on flag POF (PCON.4) will be set 1 to indicate a cold reset, a power-on process complete. Note that the contents of internal RAM will be undetermined after a power-on. It is recommended that user gives initial values for the RAM block.

The POF is recommended to be cleared to 0 via software to check if a cold reset or warm reset performed after the next reset occurs. If a cold reset caused by power off and on, POF will be set 1 again. If the reset is a warm reset caused by other reset sources, POF will remain 0. User may take a different course to check other reset flags and deal with the warm reset event. For detailed electrical characteristics, refer to the table 35-7 and 35-8.

PCON – Power Control

7	6	5	4	3	2	1	0
SMOD	SMOD0	LPR	POF	GF1	GF0	PD	IDL
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W

Address: 87H, All pagess POR reset value: 0001 000b, other reset value: 000U 0000b

Bit	Name	Description

Bit	Name	Description
4	POF	Power-on reset flag This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.

6.3.1.2 nRESET Reset Waveform

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 VDD and the state keeps longer than 32 system clock, chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 VDD and the state keeps longer than 200 us (glitch filter). The POF will be set 1. Figure 6.3-1 nRESET Reset Waveform錯誤! 找不到參照來源。 shows the nRESET reset waveform.

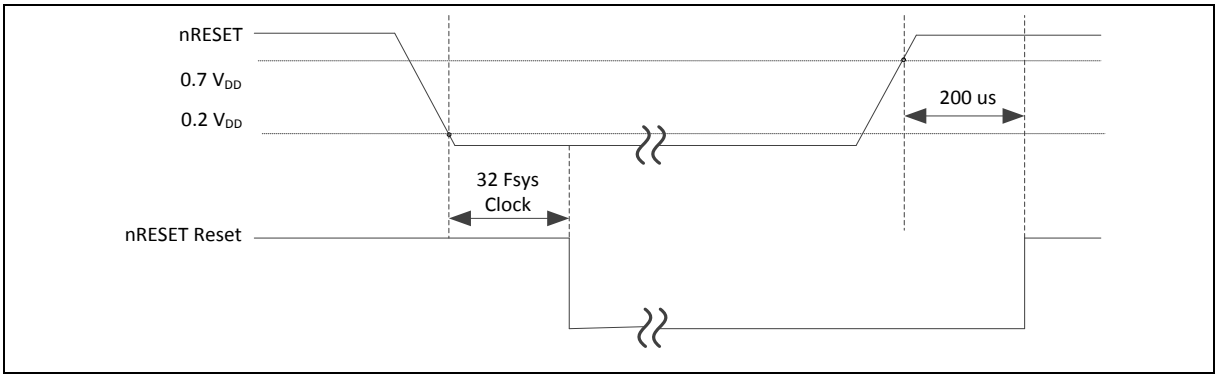


Figure 6.3-1 nRESET Reset Waveform

6.3.1.3 Low Voltage Reset (LVR) Waveform

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.3-4 shows the Low Voltage Reset waveform.

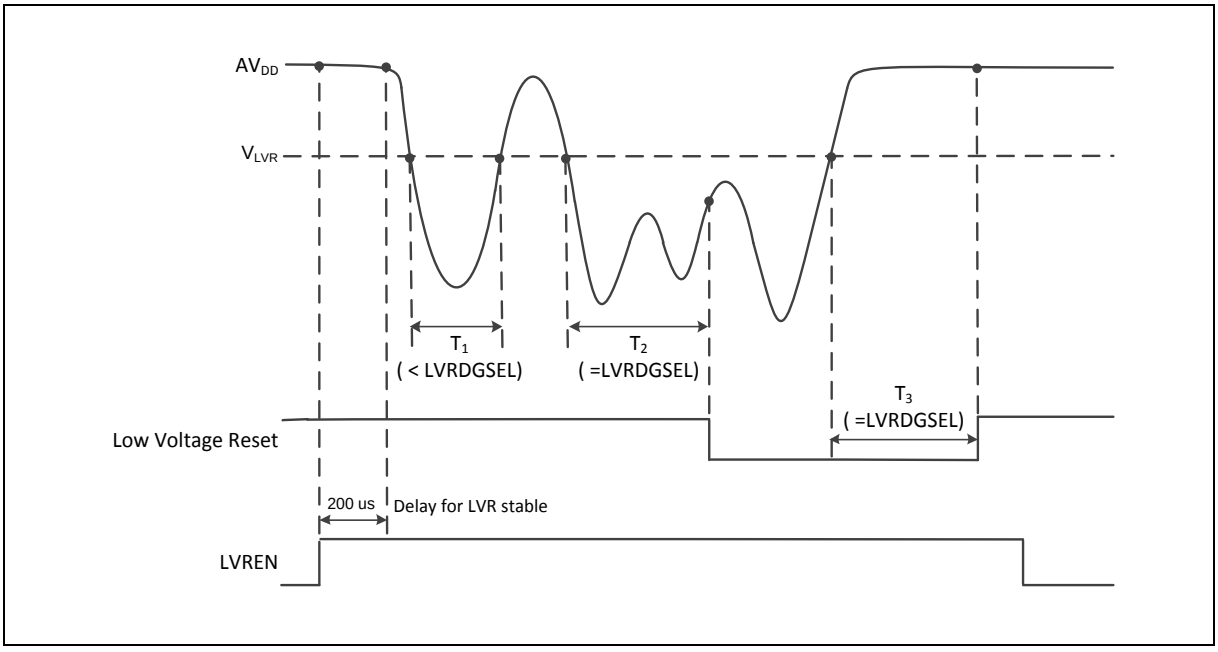


Figure 6.3-2 Low Voltage Reset (LVR) Waveform

6.3.1.4 Brown-Out Reset

The brown-out detection circuit is used for monitoring the V_{DD} level during execution. When V_{DD} drops to the selected brown-out trigger level (V_{BOD}), the brown-out detection logic will reset the MCU if BORST (BODCON0.2) setting 1. After a brown-out reset, BORF (BODCON0.1) will be set as 1 via hardware. BORF will not be altered by any reset other than a power-on reset or brown-out reset itself. This bit can be set or cleared by software.

BODCON0 – Brown-out Detection Control 0 (TA protected)

7	6	5	4	3	2	1	0
BODEN	BOV[2:0]			BOF	BORST	BORF	BOS
R/W	R/W			R/W	R/W	R/W	R

Address: A3H, Page 0 Reset value: POR: CCCC XC0Xb / BOD: UUUU XU1Xb / Others: UUUU XUUXb

Bit	Name	Description
1	BORF	Brown-out reset flag When the MCU is reset by brown-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.

6.3.1.5 External Reset and Hard Fault Reset

The external reset pin $\overline{RST}$ is an input with a Schmitt trigger. An external reset is accomplished by holding the $\overline{RST}$ pin low for at least 24 system clock cycles to ensure detection of a valid hardware reset signal. The reset circuitry then synchronously applies the internal reset signal. Thus, the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain as long as $\overline{RST}$ pin is low. After the $\overline{RST}$ high is removed, the MCU will exit the reset state and begin code executing from address 0000H. If an external reset applies while CPU is in Power-down mode, the way to trigger a hardware reset is slightly different. Since the Power-down mode stops system clock, the reset signal will asynchronously cause the system clock resuming. After the system clock is stable, MCU will enter the reset state.

There is a RSTPINF (AUXR0.6) flag, which indicates an external reset took place. After the external reset, this bit will be set as 1 via hardware. RSTPINF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software.

Hard Fault reset will occur if CPU fetches instruction address over flash size, HardF (AUXR0.5) flag will be set via hardware. HardF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software. If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled. Only HardF flag be asserted.

AUXR0 – Auxiliary Register 0

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	HardFInt	GF2	-	0	DPS
R/W	R/W	R/W	R/W	R/W	-	R	R/W

Address: A2H, Page:0
Reset value: POR: 0000 0000b / Software: 1UU0 0000b / Reset pin: U1U0 0000b / Hard fault: UU10 0000b / Others: UUU0 0000b

Bit	Name	Description
6	RSTPINF	External reset flag When the MCU is reset by the external reset, this bit will be set via hardware. It is recommended that the flag be cleared via software.
5	HardF	Hard Fault reset flag Once CPU fetches instruction address over flash size while EHFI (EIE1.4)=0, MCU will reset and this bit will be set via hardware. It is recommended that the flag be cleared via software. **Note:** If MCU run in OCD debug mode and OCDEN = 0, Hard fault reset will disable. Only HardF flag be asserted.

6.3.1.6 Watchdog Timer Reset

The WDT is a free running timer with programmable time-out intervals and a dedicated internal clock source. User can clear the WDT at any time, causing it to restart the counter. When the selected time-out occurs but no software response taking place for a while, the WDT will reset the system directly and CPU will begin execution from 0000H.

Once a reset due to WDT occurs, the WDT reset flag WDTRF (WDCON.3) will be set. This bit keeps unchanged after any reset other than a power-on reset or WDT reset itself. User can clear WDTRF via software.

WDCON – Watchdog Timer Control (TA protected)

7	6	5	4	3	2	1	0
WDTR	WDCLR	WDTF	WIDPD	WDTRF	WDPS[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W		

Address: AAH, Page 0 Reset value: POR: 0000 0111b / WDT: 0000 1UUUb / Others: 0000 UUUUb

Bit	Name	Description
3	WDTRF	WDT reset flag When the CPU is reset by WDT time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software after reset.

6.3.1.7 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.3-3 shows the power-on reset waveform.

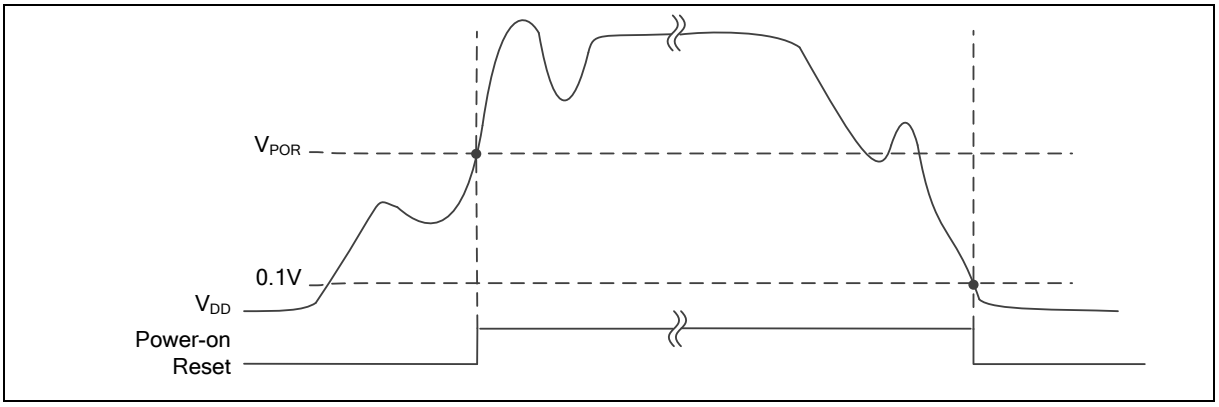


Figure 6.3-3 Power-on Reset (POR) Waveform

6.3.1.8 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.3-4 shows the Low Voltage Reset waveform.

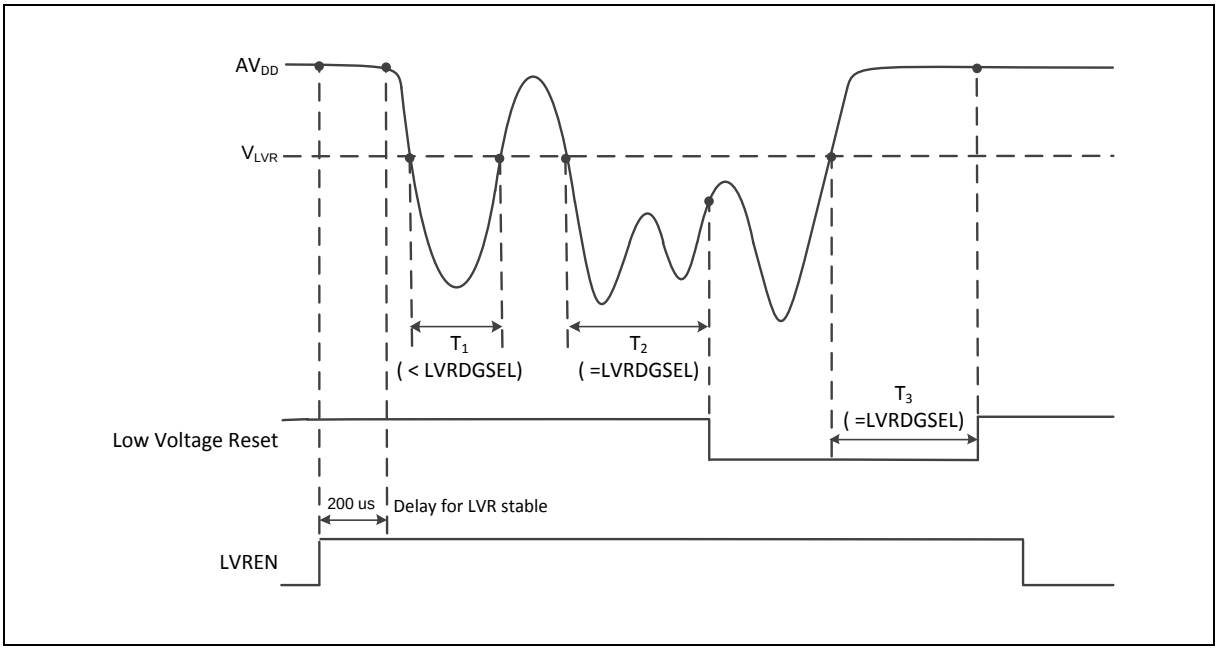


Figure 6.3-4 Low Voltage Reset (LVR) Waveform

6.3.1.9 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.3-5 shows the Brown-out Detector waveform.

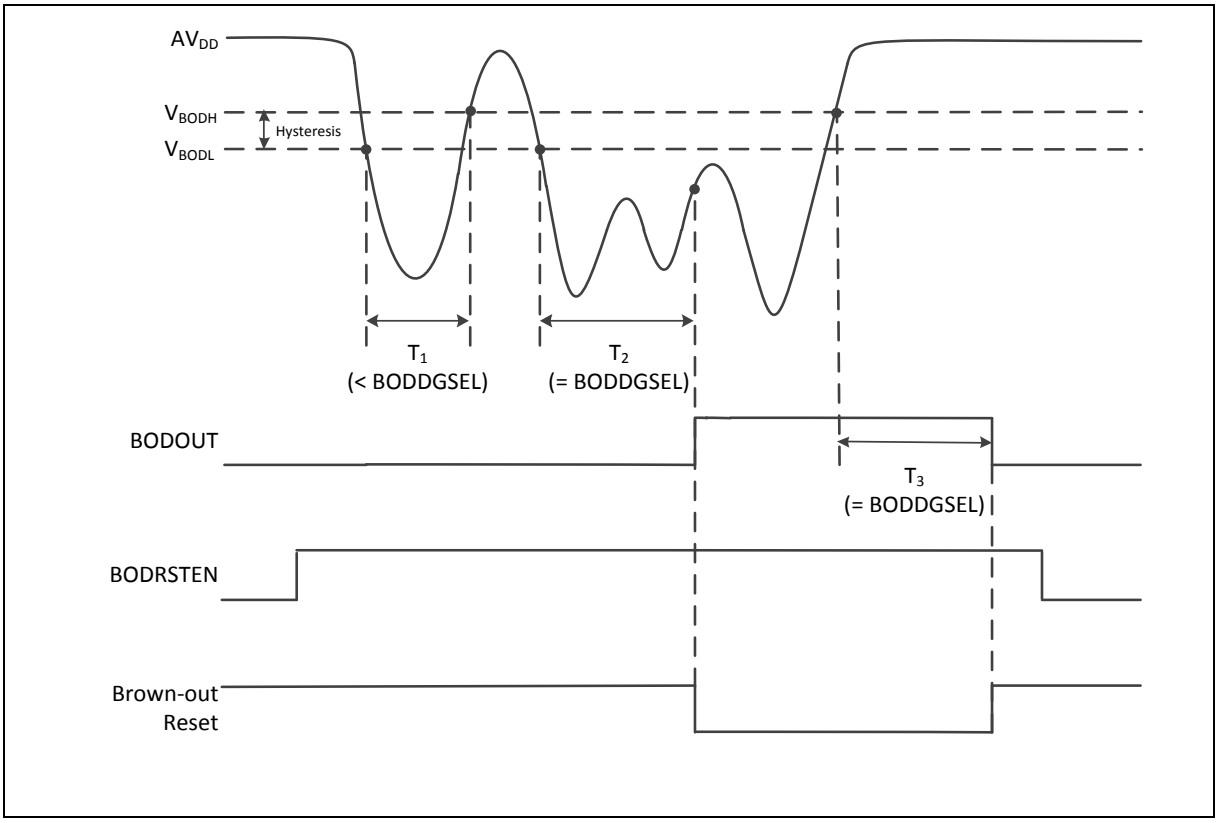


Figure 6.3-5 Brown-out Detector (BOD) Waveform

6.3.1.10 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

7 ELECTRICAL CHARACTERISTICS

7.1 General Operating Conditions

(V_{DD}-V_{SS} = 1.8 ~ 5.5V, T_A = 25°C, Fsys = 24 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	1.8	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	External Analog reference voltage	1.8	-	AV_{DD}		$AV_{DD} - V_{REF} < 1.2$ V
	Internal Analog reference voltage VRFSEL[2:0] = 001[2]	2.028V	2.048	2.068V		
	Internal Analog reference voltage VRFSEL[2:0] = 011[2]	3.052	3.072V	3.092V		
V_{BG}	Band-gap voltage[2]	0.793	0.814	0.835		T_A = -40°C ~105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.

Table 7.1-1 General operating conditions

7.2 DC Electrical Characteristics

7.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 1. 8V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz (HIRC)[1]	2.40	2.64	2.87	2.90	mA
		24 MHz (HXT) [2][5]	2.52	2.97	3.10	3.16	
		12 MHz (HXT) [2][5]	1.56	2.04	2.13	2.20	
		4 MHz (HXT) [2][5]	0.91	1.33	1.39	1.43	
		38.4 kHz (LIRC)[3]	0.22	0.29	0.32	0.35	
		32.768 kHz (LXT)[4]	0.24	0.30	0.32	0.35	
	Normal run mode, executed from Flash, all peripherals enable	24 MHz (HIRC)[1]	3.50	3.78	3.86	3.89	
		24 MHz (HXT) [2][5]	3.62	4.11	4.24	4.31	
		12 MHz (HXT) [2][5]	2.26	2.74	2.83	2.92	
		4 MHz (HXT) [2][5]	1.30	1.74	1.81	1.83	
		38.4 kHz (LIRC)[3]	0.37	0.57	0.59	0.61	
		32.768 kHz (LXT)[4]	0.40	0.58	0.60	0.62	

Notes:

1. This value base on HIRC enable, HXT disable, LIRC enable, LXT enable
2. This value base on HIRC disable, HXT enable, LIRC enable, LXT disable
3. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable
4. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable

5.	Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values
6.	AV_{DD} = V_{DD} = 3.3V, LVR17 enabled, POR enable and BOD enable.
7.	Based on characterization, not tested in production unless otherwise specified.

Table 7.2-1 Current consumption in Normal Run mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_LPRUN}	Low power run mode, executed from Flash, all peripherals disable	38.4 kHz (LIRC)[1]	15	21	42	66	µA
		32.768 kHz (LXT)[2]	19	23	44	67	
	Low power run mode, executed from Flash, all peripherals enable	38.4 kHz (LIRC)[1]	193	307	320	344	
		32.768 kHz (LXT)[2]	194	308	321	345	

Notes:

1.	This value base on HIRC disable, HXT disable, LIRC enable, LXT disable
2.	This value base on HIRC disable, HXT disable, LIRC enable, LXT enable
3.	Based on characterization, not tested in production unless otherwise specified.
4.	AV_{DD} = V_{DD} = 3.3V, LVR17 enabled, POR enable and BOD disable.

Table 7.2-2 Current consumption in Low Power Run mode

Symbol	Conditions	Fsys	Typ [6]	Max[6][7]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable	24 MHz (HIRC)[1]	1.43	1.58	1.62	1.64	mA
		24 MHz (HXT) [2][5]	1.52	1.91	2.00	2.05	
		12 MHz (HXT) [2][5]	1.07	1.44	1.50	1.56	
		4 MHz (HXT) [2][5]	0.76	1.10	1.15	1.19	
		38.4 kHz (LIRC)[3]	0.20	0.30	0.32	0.35	
		32.768 kHz (LXT)[4]	0.22	0.32	0.34	0.36	
	Idle mode, all peripherals enable	24 MHz (HIRC)[1]	2.46	2.72	2.78	2.80	
		24 MHz (HXT) [2][5]	2.55	3.04	3.15	3.19	
		12 MHz (HXT) [2][5]	1.67	2.14	2.22	2.26	
		4 MHz (HXT) [2][5]	1.08	1.51	1.57	1.60	
		38.4 kHz	0.37	0.57	0.60	0.61	

		(LIRC)[3]					
		32.768 kHz (LXT)[4]	0.38	0.59	0.61	0.62	

Notes:
1. This value base on HIRC enable, HXT disable, LIRC enable, LXT enable
2. This value base on HIRC disable, HXT enable, LIRC enable, LXT disable
3. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable
4. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable
5. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values
6. Based on characterization, not tested in production unless otherwise specified.
7. $AV_{DD} = V_{DD} = 3.3V$, LVR17 enabled, POR enable and BOD enable.

Table 7.2-3 Current consumption in Idle mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_LPIDLE}	Low power idle mode, executed from Flash, all peripherals disable	38.4 kHz (LIRC)[1]	13	19	40	63	µA
		32.768 kHz (LXT)[2]	15	20	41	65	
	Low power idle mode, executed from Flash, all peripherals enable	38.4 kHz (LIRC)[1]	173	304	317	341	
		32.768 kHz (LXT)[2]	174	306	319	342	

Notes:
1. This value base on HIRC disable, HXT disable, LIRC enable, LXT disable
2. This value base on HIRC disable, HXT disable, LIRC enable, LXT enable
3. Based on characterization, not tested in production unless otherwise specified.
4. $AV_{DD} = V_{DD} = 3.3V$, LVR17 enabled, POR enable and BOD enable.

Table 7.2-4 Current consumption in Low Power Idle mode

Symbol	Test Conditions	Typ[1]	Max[2][3]			Unit
		T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power down mode, all peripherals disable@3.3V	0.8	1.6[4]	18	34	µA
	Power down mode, all peripherals disable@5.5V	1.6	2.5	25	50	
	Power down mode, LVR enable all other peripherals disable	1.4	3.2	19	36	
	Power down mode, LVR enable BOD enable all other peripherals disable	60	80	70	100	
	Power down mode, WDT / WKT enable all use LIRC, BOD disable	2.87	5.2	21	37	
	Power down mode, WDT use LIRC, WKT use LXT, BOD disable	2.42	4.2	20	38	

Notes:

1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 enabled, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.
4. Based on characterization, tested in production.

Table 7.2-5 Chip Current Consumption in Power down mode

7.2.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- The system clock = 24 MHz.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	$I_{DD\ Base}$	I_{DD}[*1]	Unit
ADC[*2]	309.2		µA
ACMP0[*3]	1.0		
ACMP1[*3]	1.1		
PWM0	152.3		
SPI0	40.2		
SPI1	44.2		
UART0	98.8	1	
UART1		1	
I2C0	118.7	1	
I2C1		1	
SC0	67.8		
PIN Interrupt	0.2		
TIMER 0	145	4.1	
TIMER 1		3.9	
TIMER 2		4.4	
TIMER 3		10	
INT0	0.3		
INT1	0.3		
WDT	0.4		
WKT	0.7		
PDMA0	13.4	0.5	
PDMA1		0.5	
PDMA2		0.5	
PDMA3		0.5	
CAPTURE0	145	0.5	
CAPTURE1		0.3	
CAPTURE2		0.5	

Notes:

1. Guaranteed by characterization results, not tested in production.

2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 7.2-6 Peripheral Current Consumption

7.2.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 7.1-1 is measured on a wakeup phase with a 24 MHz HIRC oscillator.

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[1][2]	Wakeup from Power down mode	Fsys = HIRC @5.5V	7	20	µs
		Fsys = HIRC @1.8V	13	20	µs
		Fsys = HXT@24MHz @5.5V	370[3]	500[3]	µs
		Fsys = HXT@24MHz @1.8V	600[3]	800[3]	µs
		Fsys = LIRC @5.5V	938	1500	µs
		Fsys = LIRC @1.8V	938	1500	µs
		Fsys = LXT@32.768KHz @5.5V	860[4]	1000[4]	µs
		Fsys = LXT@32.768KHz @1.8V	860[4]	1000[4]	µs

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first
3. Value variable based on extnerl Crystal stable time.
4 Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values, LXT not disabled when ML51 into Power down mode.

Table 7.2-7 Low-power mode wakeup timings

7.2.4 I/O DC Characteristics

7.2.4.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode
R_{PU}[*1] [*3]	Pull up resistor	40	-	60	kΩ	V_{DD} = 5.5 V, Quasi mode and Input mode with pull up enable
		40	-	60		V_{DD} = 3.3 V, Quasi mode and Input mode with pull up enable
		40	-	70		V_{DD} = 1.8 V, Quasi mode and Input mode pull up enable
R_{PD}[*1] [*3]	Pull down resistor	40	-	60	kΩ	V_{DD} = 5.5 V, Quasi mode and Input mode with pull up enable
		40	-	60		V_{DD} = 3.3 V, Quasi mode and Input mode with pull up enable
		40	-	70		V_{DD} = 1.8 V, Quasi mode and Input mode pull up enable

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 7.2-8 I/O input characteristics

7.2.4.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.7	-7.8	-8	µA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.7	-7.8	-8	µA	V_{DD} = 4.5 V V_{IN} =(V_{DD}-0.4) V
		-7.6	-7.8	-7.9	µA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.6	-7.8	-7.9	µA	V_{DD} = 2.5 V V_{IN} =(V_{DD}-0.4) V
		-7.6	-7.7	-7.8	µA	V_{DD} = 1.8 V V_{IN} =(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-8.7	-9	-9.4	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.4	-7.8	-8.1	mA	V_{DD} = 4.5 V V_{IN} =(V_{DD}-0.4) V
		-5.6	-5.7	-6.2	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.4	-4.8	-5.0	mA	V_{DD} = 2.5 V V_{IN} =(V_{DD}-0.4) V
		-2.4	-2.6	-3.0	mA	V_{DD} = 1.8 V V_{IN} =(V_{DD}-0.4) V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	20	22	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		18	19	20	mA	V_{DD} = 4.5 V V_{IN} = 0.4 V
		14	15	16	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		11	12	13	mA	V_{DD} = 2.5 V V_{IN} = 0.4 V
		6	7	8.3	mA	V_{DD} = 1.8 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 7.2-9 I/O output characteristics

7.2.4.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		50	-	65		V_{DD} = 1.8 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:
1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 7.2-10 nRESET Input Characteristics

7.3 AC Electrical Characteristics

7.3.1 24 MHz Internal High Speed RC Oscillator (HIRC)

The 24 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	5.5	V	
F_{HRC}	Oscillator frequnecy	23.76	24	24.24	MHz	T_A = 25 °C, V_{DD} = 5V
	Frequency drift over temperarure and volatge	-1[1]	-	1[1]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[2]	-	2[2]	%	T_A = -20°C ~ +105 °C, V_{DD} = 1.8 ~ 5.5V
		-5[2]		5[2]	%	T_A = -40°C ~ -20°C, V_{DD} = 1.8 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 5.5V

Notes:
1. Based on characterization, tested in production.
2. Guaranteed by characterization result, not tested in production.
3. Guaranteed by design.

Table 7.3-1 24 MHz Internal High Speed RC Oscillator(HIRC) characteristics

7.3.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	38.4	-	kHz	
	Frequency drift over temperarure and volatge	-2[1]	-	2[1]	%	T_A = 25 °C, V_{DD} = 5V
		-10[2]	-	10[2]	%	T_A=-40~105°C V_{DD}=1.8V~5.5V Without software calibration
I_{LRC} [2]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C V_{DD}=1.8V~5.5V

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. The 38.4 kHz low speed RC oscillator can be calibrated by user.
4. Guaranteed by design.

Table 7.3-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

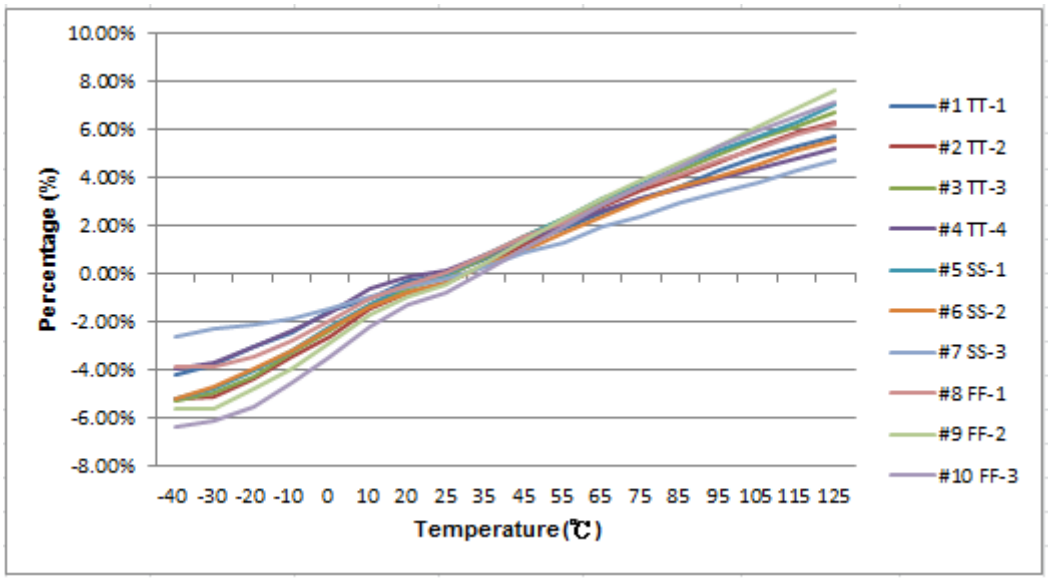


Figure 7.3-1 LIRC deviation under V_{DD} = 5.5 V

7.3.3 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions[2]
V_{DD}	Operating voltage	1.8	-	5.5	V	
R_f	Internal feedback resister	-	500	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	80	180	µA	4 MHz, Gain = L0
		-	110	300		8 MHz, Gain = L1
		-	180	500		12 MHz, Gain = L2
		-	230	650		16 Mhz, Gain = L3
		-	360	975		24 MHz, Gain = L4
T_S	Stable time	-	3500	3700	µs	4 MHz, Gain = L0
		-	950	1050		8 MHz, Gain = L1
		-	700	850		12 MHz, Gain = L2
		-	450	550		16 Mhz, Gain = L3
		-	400	570		24 MHz, Gain = L4
Du_{HXT}	Duty cycle	40	-	60	%	

Notes:
1. Guaranteed by characterization, not tested in production.
2. L0 ~ L4 defined by SFR XLTCON[6:4] HXSG

Table 7.3-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

7.3.3.2 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 25 pF	10 ~ 25 pF	without

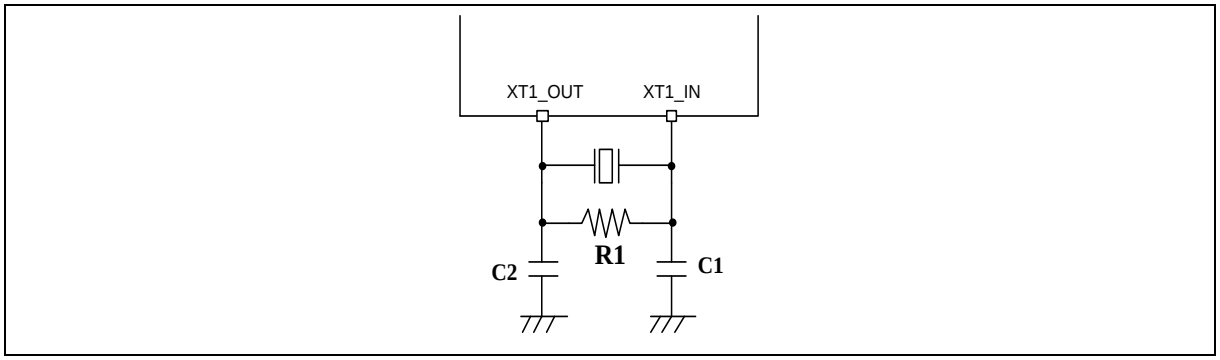
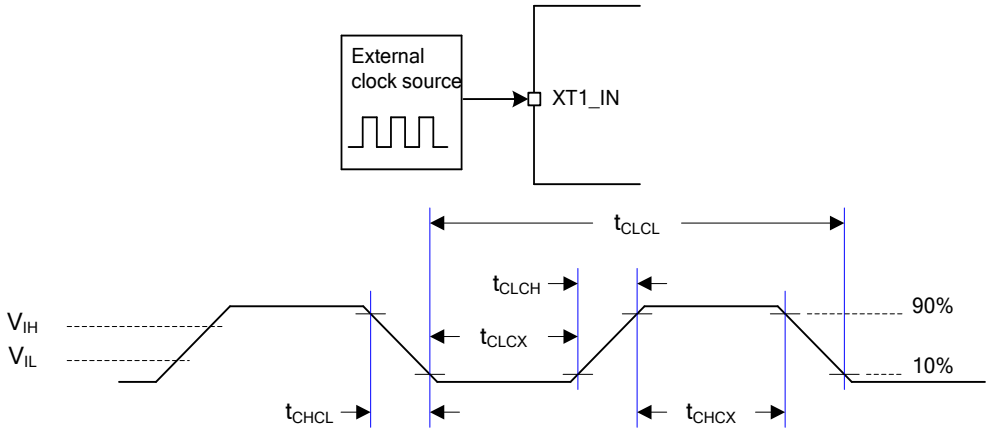


Figure 7.3-2 Typical Crystal Application Circuit

7.3.4 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.

Table 7.3-4 External 4~24 MHz High Speed Clock Input Signal

7.3.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions[2]
V_{DD}	Operation voltage	1.8	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	6	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	1.3	3.7	μA	ESR=35 kΩ, Gain = L2
		-	1.6	6		ESR=70 kΩ, Gain = L3
Ts_{LXT}	Stable time	-	2	3	s	
Du_{LXT}	Duty cycle	30	-	70	%	

Notes:
1. Guaranteed by characterization, not tested in production.
2. L1 ~ L2 defined by SFR XLTCON[1:0] LXSG

Table 7.3-5 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 7.3-6 External 32.768 kHz Low Speed Crystal Characteristics

7.3.5.2 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	20 pF	20 pF	without

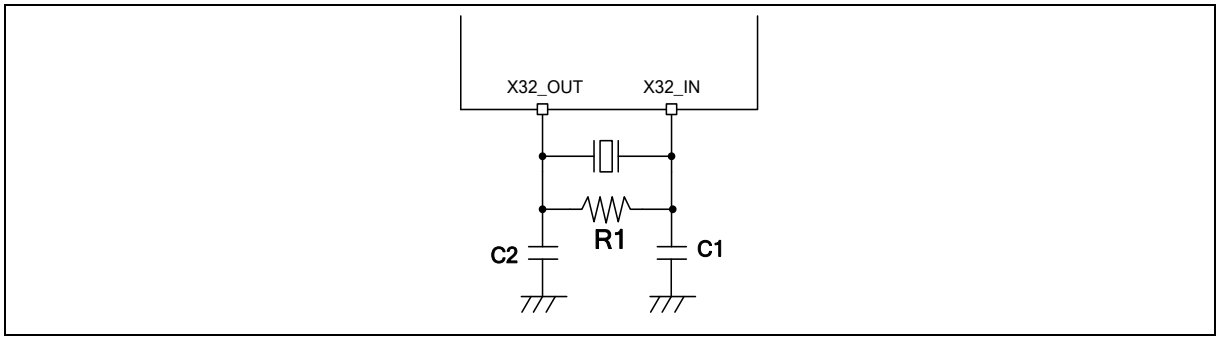
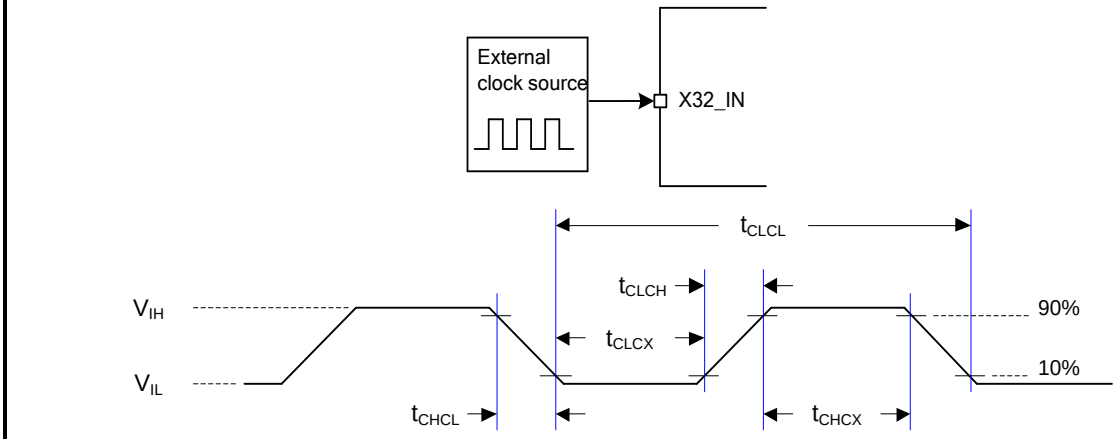


Figure 7.3-3 Typical 32.768 kHz Crystal Application Circuit

7.3.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by design, not tested in production

Table 7.3-7 External 32.768 kHz Low Speed Clock Input Signal

7.3.7 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 1.8 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 1.8 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 1.8 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 1.8 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(IO)out}$ [*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 1.8 V
					C_L = 10 pF, V_{DD} >= 1.8 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 7.3-8 I/O AC characteristics

7.4 Analog Characteristics

7.4.1 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	60	100	µA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	-	30	80		AV_{DD} = 5.5V
	LVR low power run mode operating current		0.5	1		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR reset voltage	1.45	1.55	1.65	V	-
V_{LVR}	LVR reset voltage	1.55	1.63	1.70		-
V_{BOD}	BOD brown-out detect voltage	1.7	1.8	2		V_{BOD0}
		1.9	2	2.2		V_{BOD1}
		2.3	2.4	2.5		V_{BOD2}
		2.55	2.7	2.8		V_{BOD3}
		2.85	3	3.2		V_{BOD4}
		3.55	3.7	3.9		V_{BOD5}
		4.2	4.4	4.5		V_{BOD6}
T_{LVR_SU}[*1]	LVR startup time	-	1	2	µs	-
T_{LVR_RE}[1]	LVR respond time	-	15	20		-
	LVR low power run mode respond time	-	20	30		-
T_{BOD_SU}[1]	BOD startup time	-	250	350		-
T_{BOD_RE}[1]	BOD respond time	-	19	30		-

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 7.4-1 Reset and power control unit

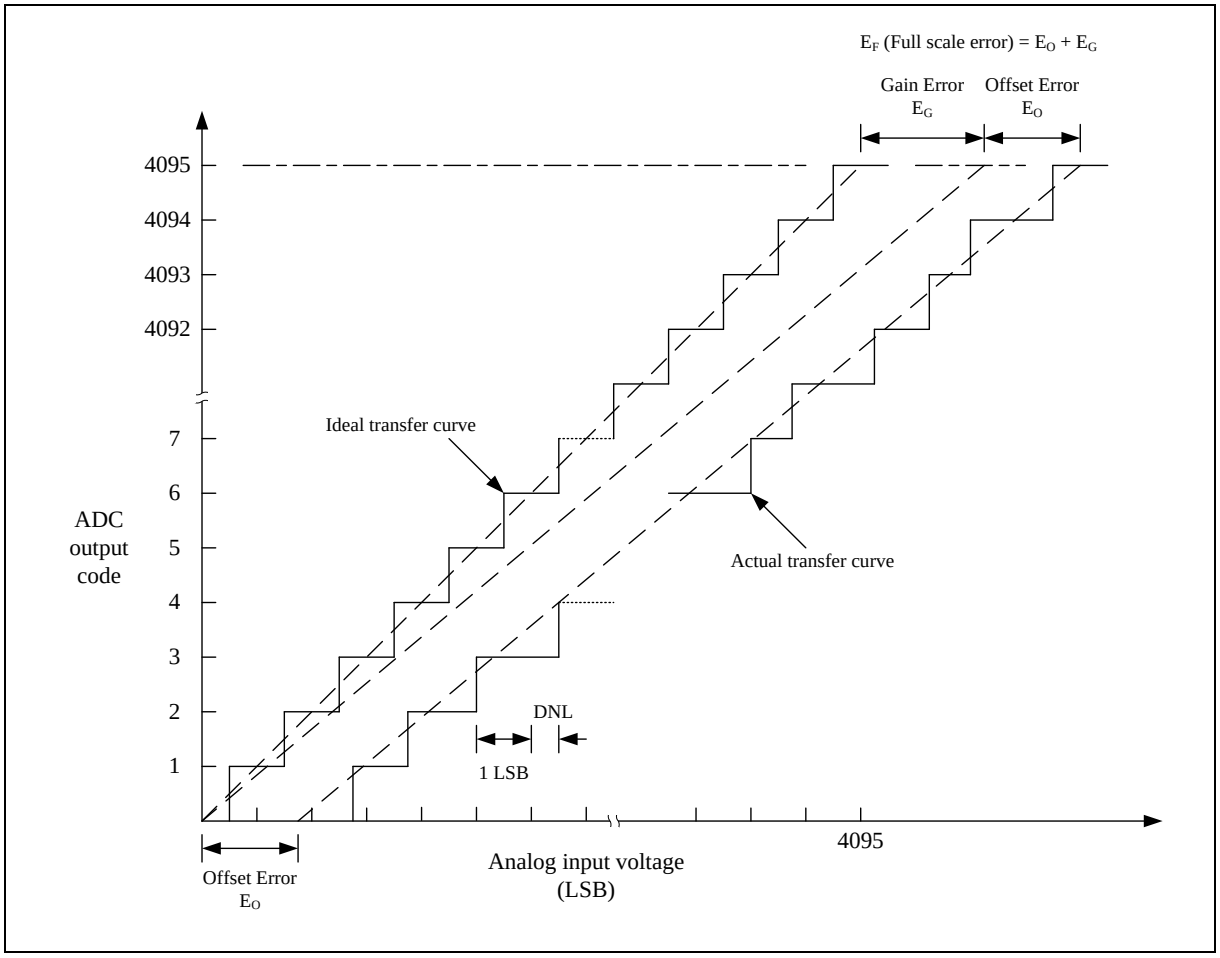
7.4.2 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	1.8	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.8	-	AV_{DD}	V	$AV_{DD} - V_{REF} < 1.2$ V
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current ($AV_{DD} + V_{REF}$ current)	-	-	360	μA	$AV_{DD} = V_{DD} = V_{REF} = 5$ V F_{ADC} = 500kHz
N_R	Resolution	10			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency		500		MHz	
T_{SMP}	Sampling Time	1	-	38	$1/F_{ADC}$	$T_{SMP} = \frac{4 * ADCAQT + 10}{F_{ADC}}$
T_{CONV}	Conversion time	1	-	128	$1/F_{ADC}$	
T_{EN}	Enable to ready time	20	-	-	μs	
INL[*1]	Integral Non-Linearity Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-2	-	+4.5	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	-3.5	-	+0.4	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-2	-	+2.5	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	-7		+7	LSB	$V_{REF} = AV_{DD}$

Notes:

1. Guaranteed by characterization result, not tested in production.

Table 7.4-2 ADC characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.4.3 Analog Comparator Controller (ACMP)

The maximum values are obtained for VDD = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	-	5.5	V	$V_{DD} = AV_{DD}$
T_A	Temperature	-40	-	105	℃	
I_{DD}	Operating current	-	2	5	μA	
V_{CM}[*2]	Input common mode voltage range	0.35	1/2 AV_{DD}	AV_{DD} -0.3		
V_{DI}[*2]	Differential input voltage sensitivity	10	20	-	mV	Hysteresis disable
V_{offset}[*2]	Input offset voltage	-	10	20	mV	Hysteresis disable
V_{hys}[*2]	Hysteresis window	-	10	20	mV	
A_v[*1]	DC voltage Gain	45	65	75	dB	
T_d[*2]	Propagation delay	-	-	5	μS	
T_{Stable}[*2]	Stable time	-	-	5	μS	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	AVDD x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	4.5	-	kΩ	
T_{SETUP_CRV}[*2]	Stable time	-	-	2	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	2	-	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 7.4-3 ACMP characteristics

7.5 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25℃
T_{ERASE}	Page erase time	-	5	-	ms	
T_{PROG}	Program time	-	10	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[3] T_A = 55℃
		25	-	-	year	100 kcycle[3] T_A = 85℃
		10	-	-	year	100 kcycle[3] T_A = 105℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 7.5-1 Flash memory characteristics

7.6 Absolute Maximum Ratings

Volrage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

7.6.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	5.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Notes:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 7.6-1 Voltage characteristics

7.6.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 7.6-2 Current characteristics

7.6.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 10-pin MSOP(3x3 mm)	-	160	-	℃/Watt
	Thermal resistance junction-ambient 14-pin TSSOP(4.4x5 mm)	-	100	-	℃/Watt
	Thermal resistance junction-ambient 20-pin QFN(3x3 mm)	-	68	-	℃/Watt
	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	℃/Watt
	Thermal resistance junction-ambient 20-pin SOP(300mil)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 28-pin TSSOP(4.4x9.7 mm)	-	30	-	℃/Watt
	Thermal resistance junction-ambient 28-pin SOP(300 mil)	-	55	-	℃/Watt
	Thermal resistance junction-ambient 32-pin LQFP(7x7 mm)	-	62	-	℃/Watt
	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)	-	28	-	℃/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 7.6-3 Thermal characteristics

7.6.4 EMC Characteristics

7.6.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

7.6.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

7.6.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8000	-	+8000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-400	-	+400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4	-	+4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 7.6-4 EMC characteristics

7.6.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
10-pin MSOP(3x3 mm) [*1]	MSL 3
14-pin TSSOP(4.4x5 mm) [*1]	MSL 3
20-pin QFN(3x3 mm) [*1]	MSL 3
20-pin TSSOP(4.4x6.5 mm) [*1]	MSL 3
20-pin SOP(300mil) [*1]	MSL 3
28-pin TSSOP(4.4x9.7 mm) [*1]	MSL 3
28-pin SOP(300 mil) [*1]	MSL 3
32-pin LQFP(7x7 mm) [*1]	MSL 3
33-pin QFN(4x4 mm) [*1]	MSL 3
48-pin LQFP(7x7 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 7.6-5 Package Moisture Sensitivity(MSL)

7.6.6 Soldering Profile

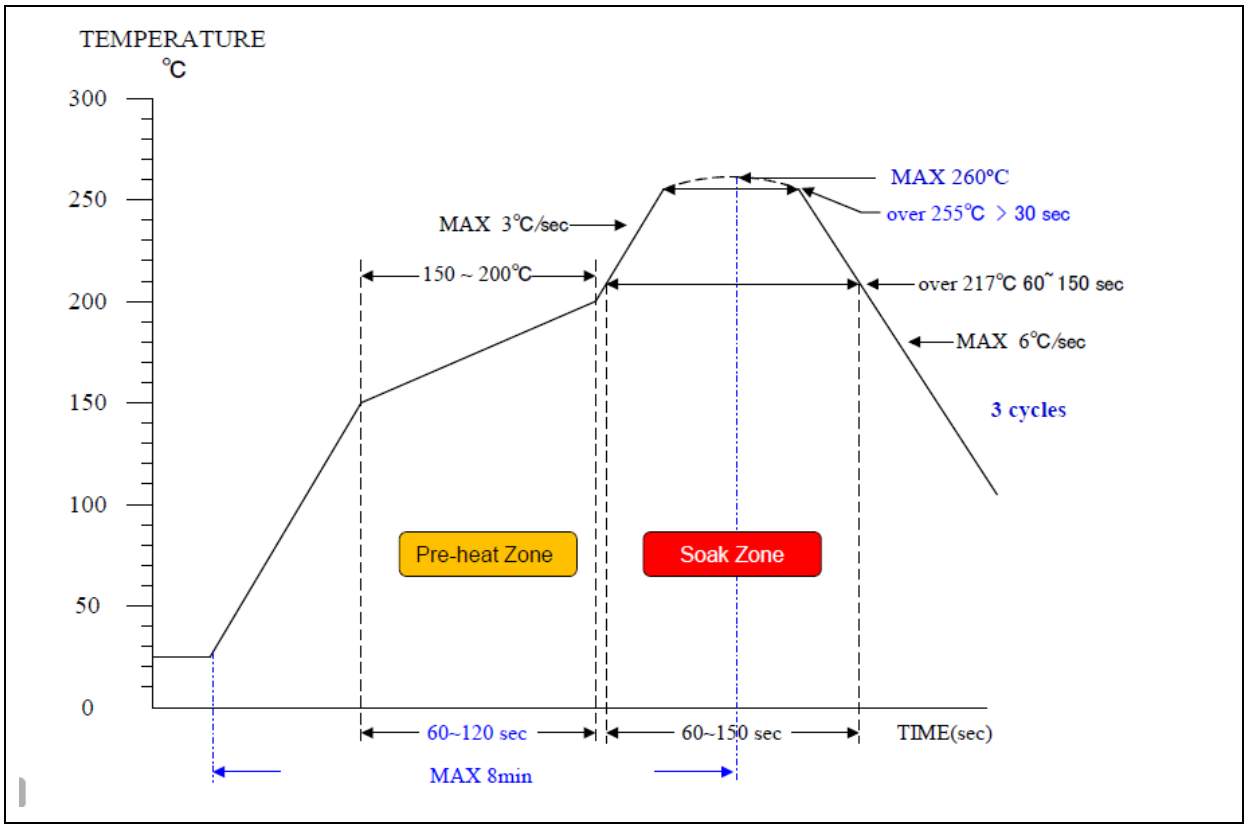


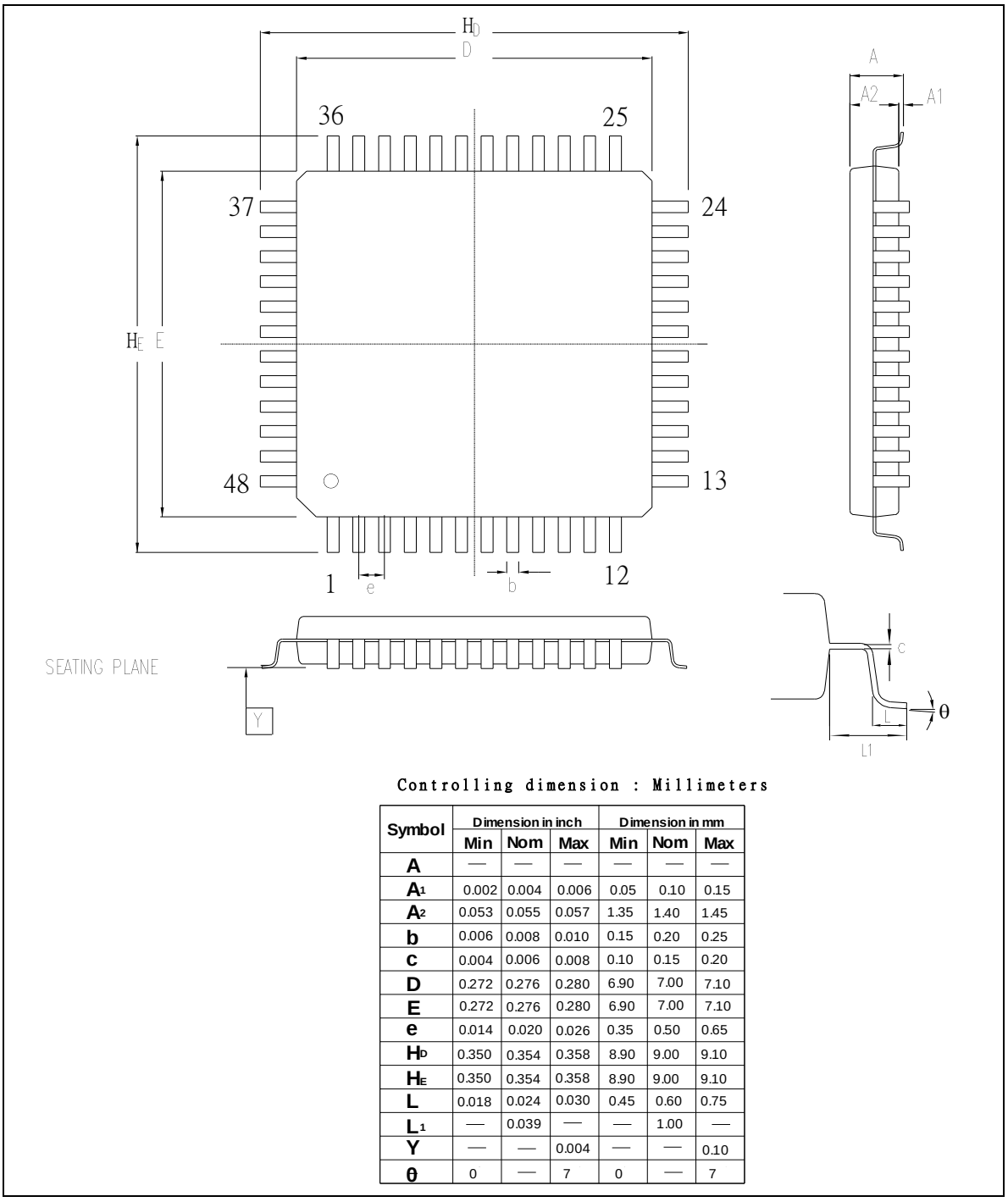
Figure 7.6-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 7.6-6 Soldering Profile

8 PACKAGE DIMENSIONS

8.1 LQFP 48 (7x7x1.4 mm)

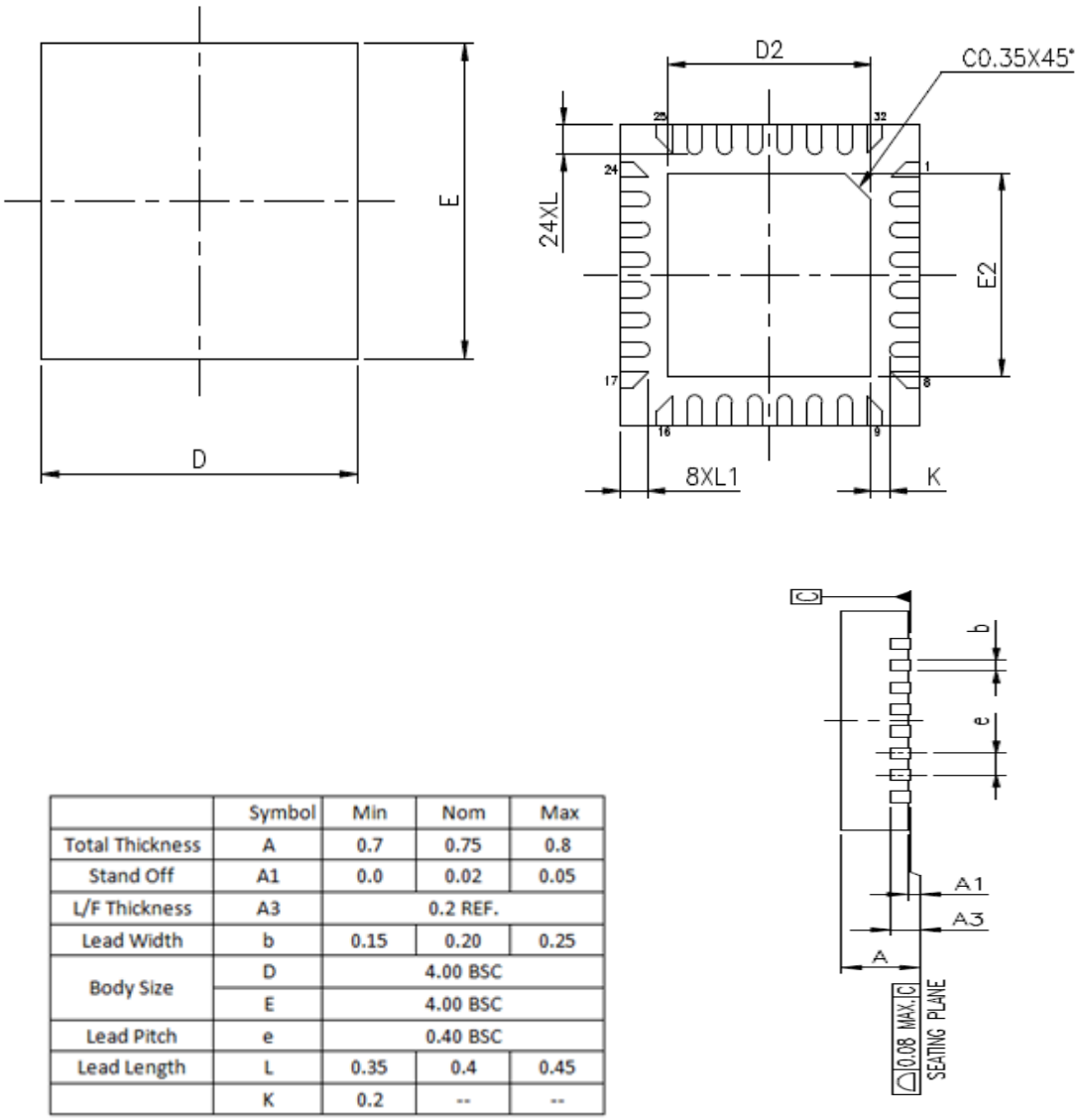


Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

Figure 8.1-1 LQFP-48 Package Dimension

8.2 QFN 33 (4x4x0.8 mm)

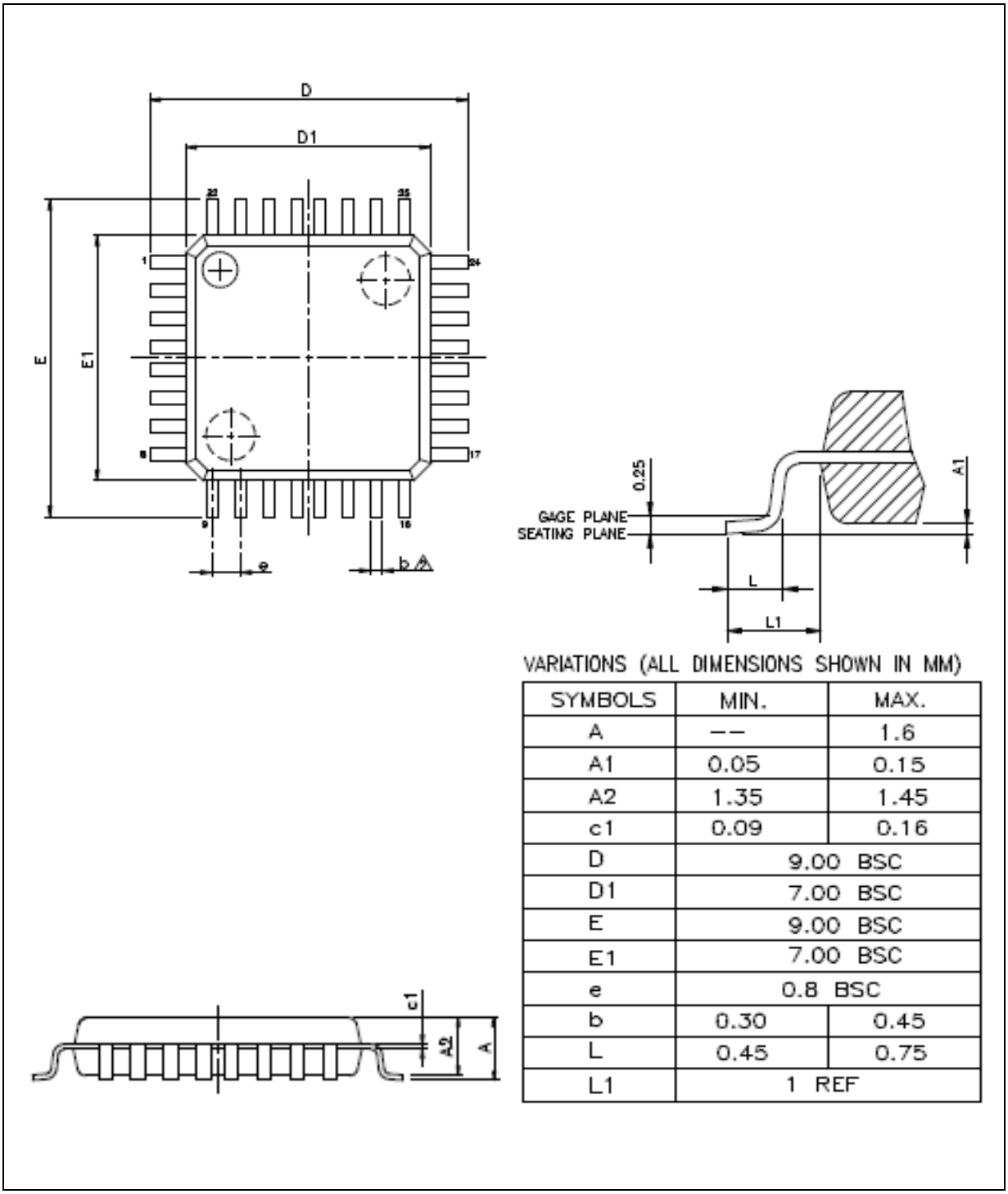


	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75

Figure 8.2-1 QFN-33 Package Dimension

8.3 LQFP 32 (7x7x1.4 mm)

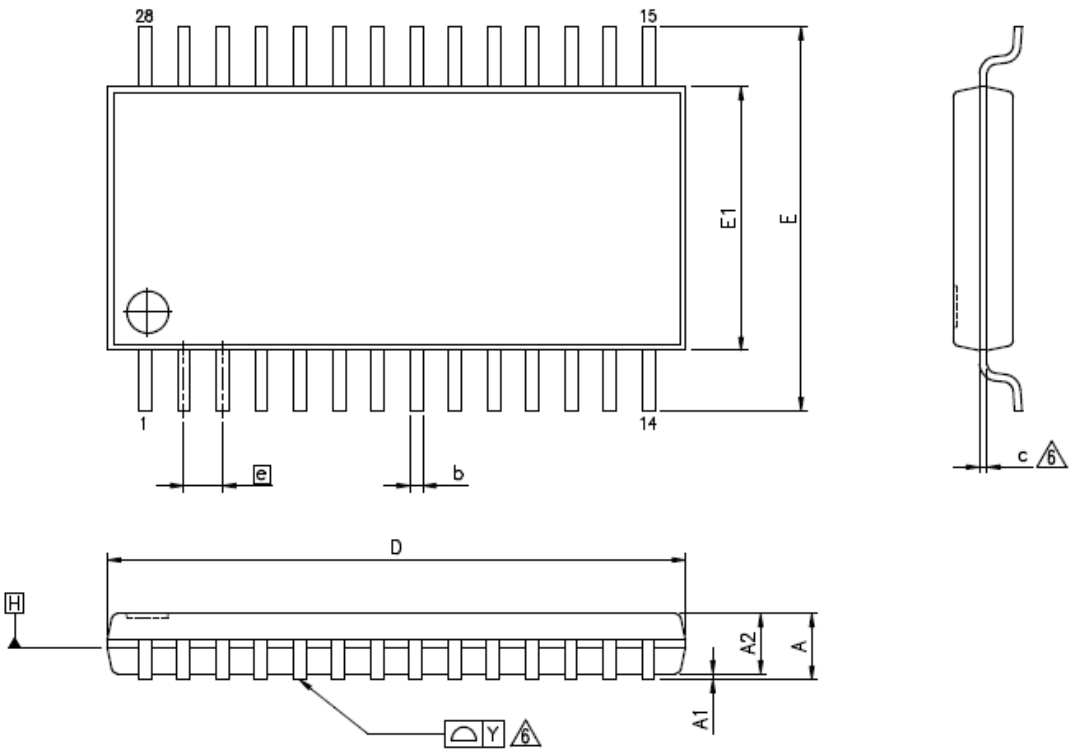


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.8 BSC	
b	0.30	0.45
L	0.45	0.75
L1	1 REF	

Figure 8.3-1 LQFP-32 Package Dimension

8.4 TSSOP 28 (4.4x9.7x1.0 mm)

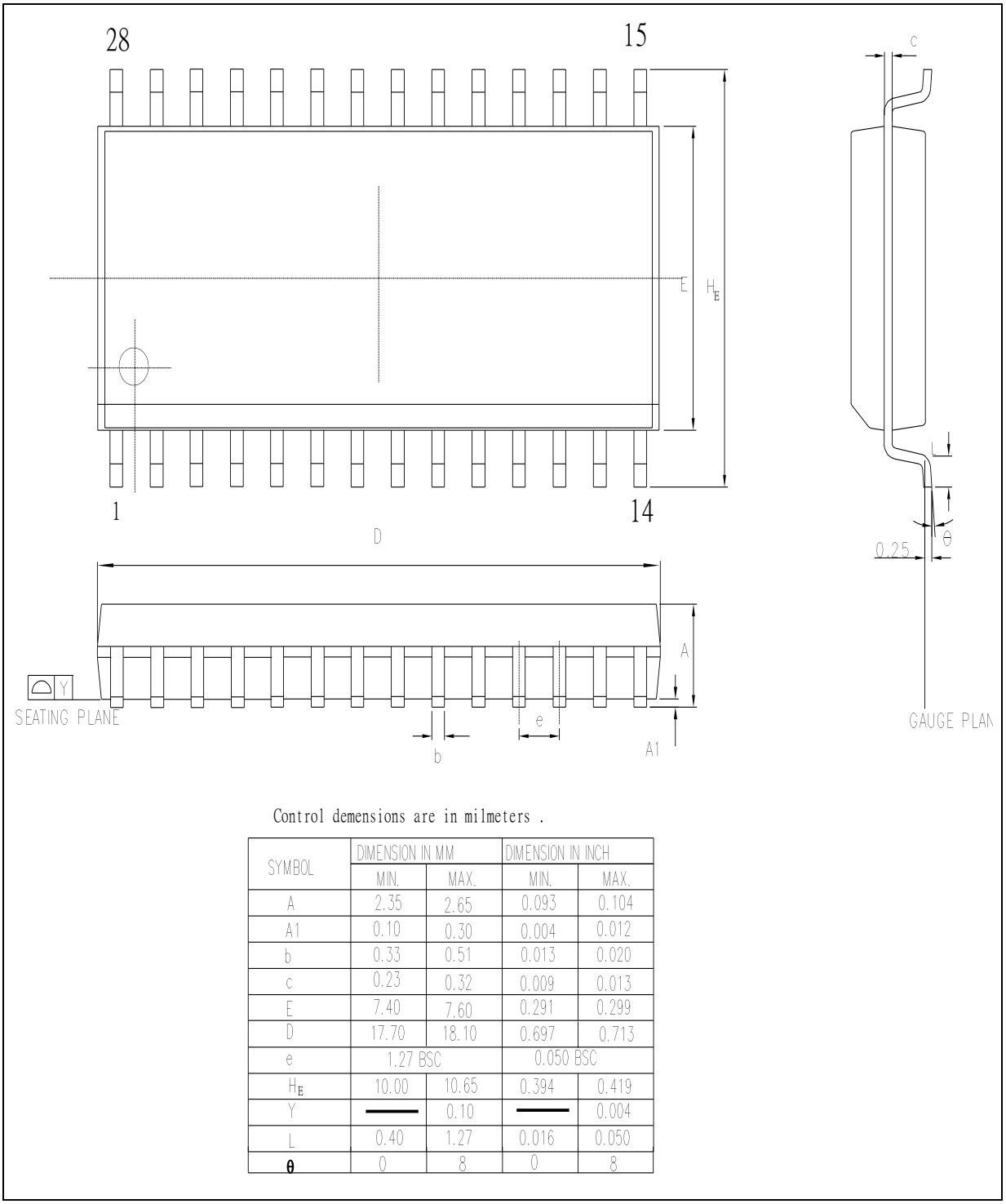


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

Figure 8.4-1 TSSOP-28 Package Dimension

8.5 SOP 28 (300 mil)

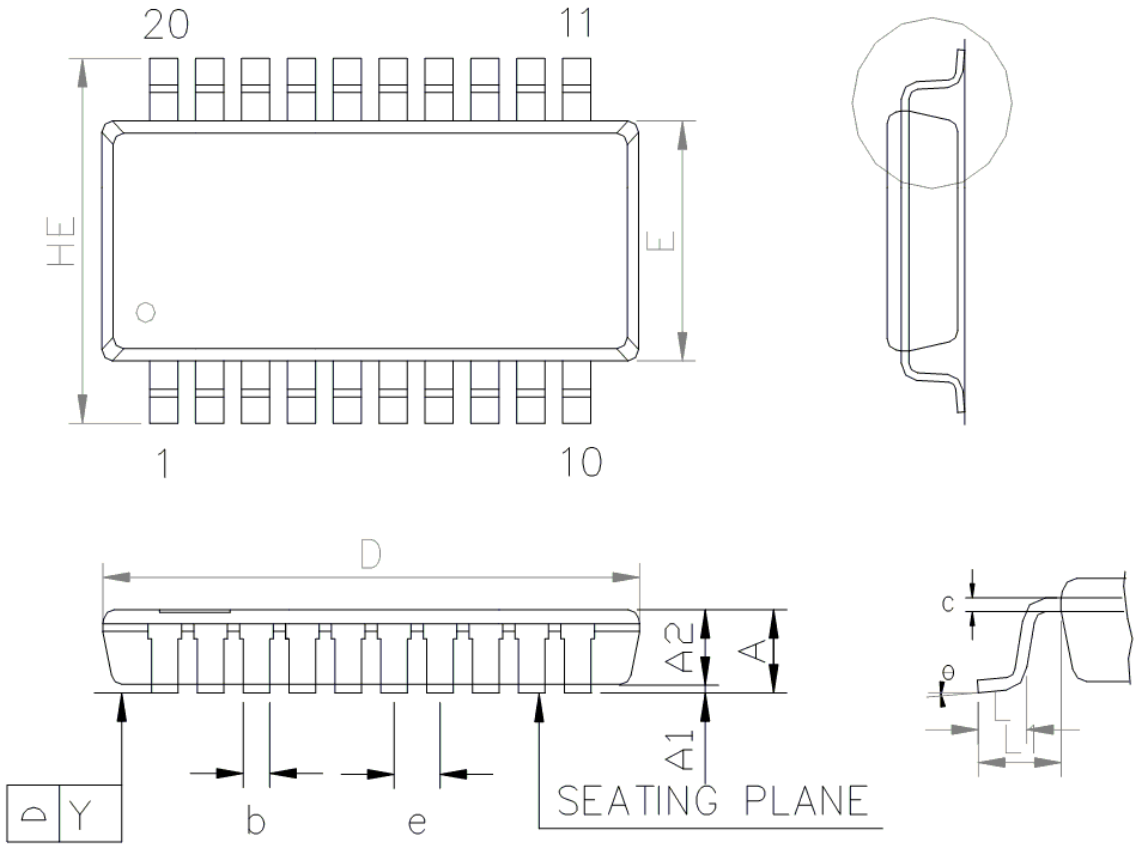


Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	17.70	18.10	0.697	0.713
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

Figure 8.5-1 SOP-28 Package Dimension

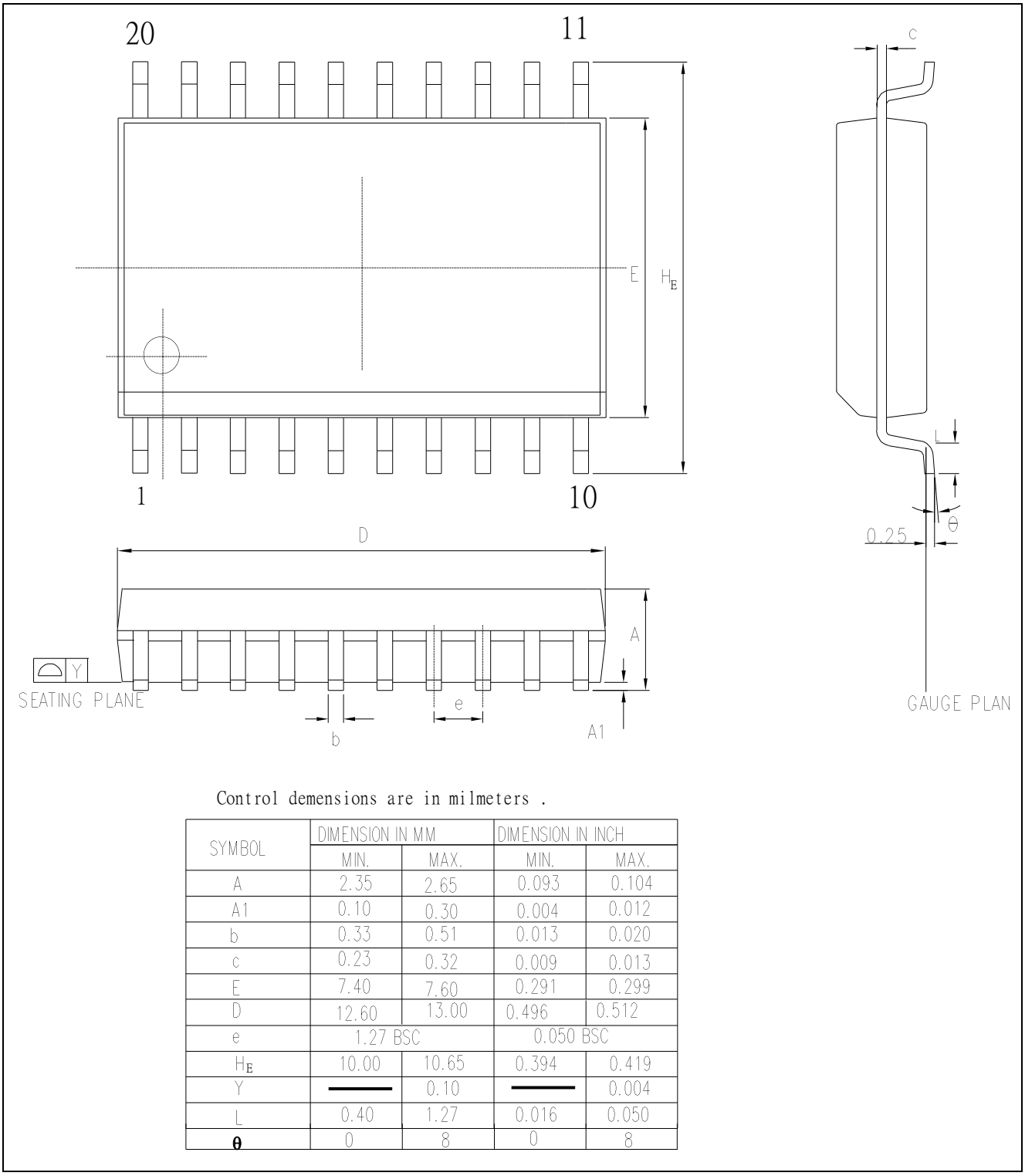
8.6 TSSOP 20 (3.0X3.0 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1,20	-	-	0.047
A1	0,05	-	0,15	0.002	-	0.006
A2	0.80	0.90	1,05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

Figure 8.6-1 TSSOP-20 Package Dimension

8.7 SOP 20 (300 mil)

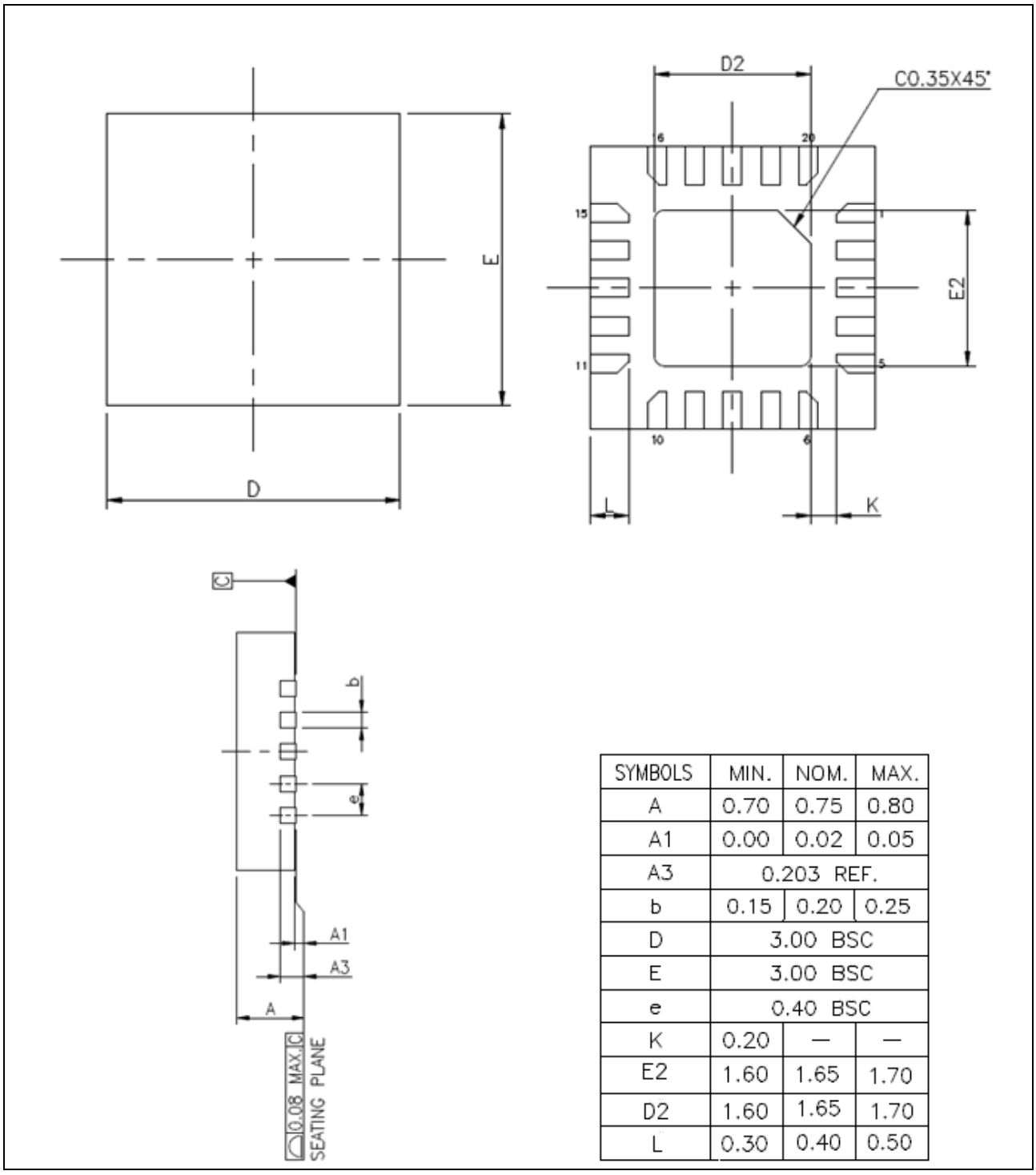


Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

Figure 8.7-1 SOP-20 Package Dimension

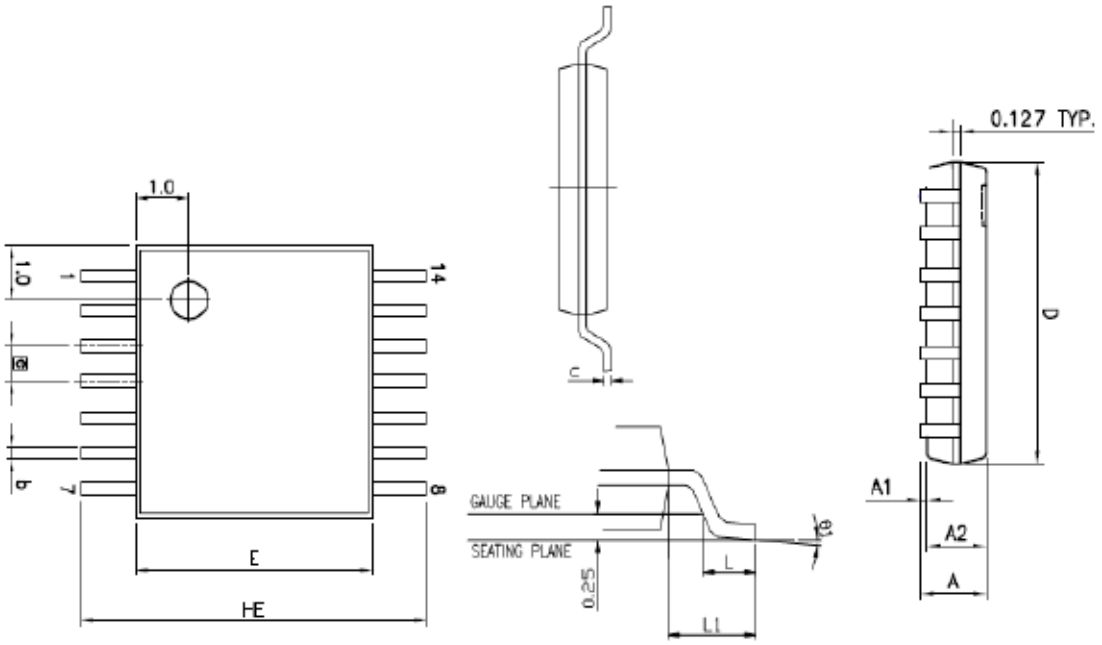
8.8 QFN 20 (3.0 X 3.0 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
e		0.40 BSC	
K	0.20	—	—
E2	1.60	1.65	1.70
D2	1.60	1.65	1.70
L	0.30	0.40	0.50

Figure 8.8-1 QFN-20 Package Dimension

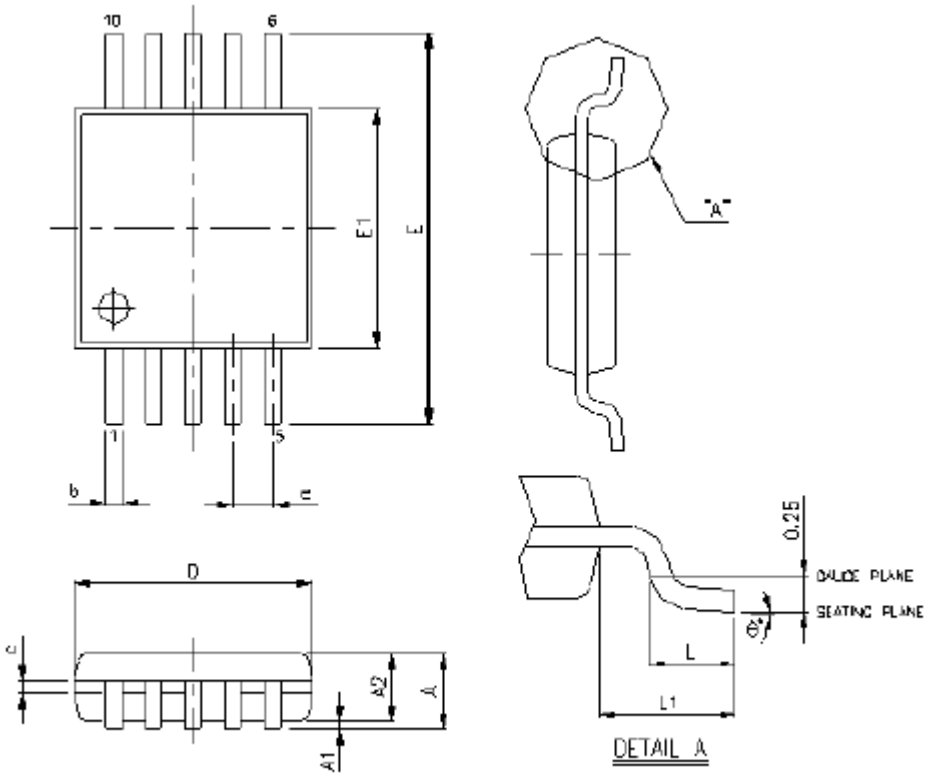
8.9 TSSOP 14 (4.4 X 5.5 mm)



CONTROLLING DIMENSION: MILLMETERS						
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.20	---	---	0.043
A1	0.05	---	0.15	0.02	---	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.50	0.60	0.75	0.020	0.024	0.030
HE	6.40 BSC.			0.252 BSC.		
E	4.30	4.40	4.50	0.169	0.173	0.177
D	4.90	5.00	5.10	0.193	0.197	0.201
b	0.19	---	0.30	0.007	---	0.012
c	0.09	---	0.20	0.004	---	0.008
L1	1.0 REF.			0.039 REF.		
e	0.65 BSC.			0.026 BSC.		
θ1	0	---	8	0	---	8

Figure 8.9-1 TSSOP-14 Package Dimension

8.10 MSOP 10 (3 x 3 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
b	0.17	–	0.27
c	0.08	–	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
θ°	0	–	8

UNIT : MM

Figure 8.10-1 MSOP-10 Package Dimension

9 ABBREVIATIONS

9.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage $eset
PDMA	Peripheral Direct Memory Access
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 9.1 List of Abbreviations

10 REVISION HISTORY

Date	Revision	Description
2018.12.05	1.00	Initial release.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.