ARM Cortex™-M4F

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC440 Product Brief

ARM® Cortex™-M4F MCU with DSP and FPU, 256/512 Kbytes Flash Memory, 64 Kbytes SRAM, 84 MHz Speed, USB OTG/HS Device, Serial Interfaces and Crypto Accelerators

For additional information or questions, please contact: Nuvoton Technology Corporation.

1 GENERAL DESCRIPTION

The NuMicro™ NUC440 series 32-bit microcontroller is embedded with ARM® Cortex™-M4F core for industrial control and applications which need high density memories and rich communication interfaces.

The NuMicro™ NUC440 Connectivity series with embedded Cortex™-M4F core with DSP extensions and a Floating Point Unit runs up to 84 MHz with 256K/512 Kbytes embedded flash memories and 64 Kbyte embedded SRAM. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timers, RTC, PDMA, EBI, UART, Smart Card Interface, SD Host, SPI, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, PS/2, 12-bit ADC, Analog Comparator, Operational Amplifier, Temperature Sensor, Low Voltage Reset Controller and Brown-out Detector. The NUC440 also provides USB 2.0 full-speed Device/Host/OTG, USB 2.0 HS device and security functions such as tamper detection, symmetric cryptographic accelerator and secure Hash function accelerator.

The NuMicro™ NUC440 Connectivity series is suitable for a wide range of applications such as:

- Industrial Automation
- PLCs
- Inverters
- Home Automation
- Security Alarm System
- Power Metering
- Portable Data Collector
- Portable RFID Reader
- System Supervisors
- USB Accessories
- Smart Card Reader
- Printer
- Motor Control

2 FEATURES

2.1 NuMicro™ NUC440 Features

- Core
  - ARM® Cortex™-M4 core running up to 84 MHz
  - Supports DSP extensions
    - Supports hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports low power sleep mode
    - Supports both WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports Nested Vectored Interrupt Controller (NVIC)
    - Supports programmable 256 level priorities for interrupts
  - Supports programmable maskable interrupts
- Build-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 256K/512 Kbytes Flash memory
  - Configurable program code/data allocation
  - ISP loader sizes 16 KB for boot code
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports In-system program (ISP), In application program (IAP) update
  - 2 Kbytes page erase for flash
  - Supports fast parallel programming mode by external programmer
- SRAM
  - 64 Kbytes embedded SRAM
  - 24 Kbytes SRAM with hardware parity check
  - Supports byte-, half-word- and word-access parity check
  - Supports NMI for parity check errors
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 16 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: fixed-priority and round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports auto increment of source and destination address
  - Supports 16-level FIFO
  - Supports bus abort status flag
  - Supports time out status flag
- Clock Control
  - Internal 22.1184 MHz high speed RC oscillator for system operation (variation < 2% at -40˚C ~ +105 ˚C)
  - Internal 10 kHz low speed RC oscillator for Watchdog Timer and Wake-up operation
  - Built-in 4~24 MHz high speed oscillator for external crystal input for precise timing operation
  - Built-in 32.768 kHz low speed oscillator for external crystal input for RTC function and low power system operation
  - Supports one PLL, up to 84 MHz for high performance system operation, sourced from
    - 22.1184 MHz internal high speed RC oscillator

- 4~24 MHz external high speed crystal oscillator
- Supports clock failure detection for system clock
- Supports exception (NMI) for clock failure detections
- Supports clock out
  - Supports 8-bit scale
  - Clock sources selectable from CPU clock or SPI clock.
- CPU clock source can be selected from USB PHY embedded PLL

- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level trigger setting
  - High driver and high sink IO mode support (To source 20mA and sink 15mA at 5V)
  - Supports up to 114/101/77/45 GPIOs for LQFP144/128/100/64, respectively.
- Timer x4
  - Supports four sets of 32-bit timers with 24-bit up-timers and 8-bit pre-scale counters
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function to count the event from external pins
  - Supports input capture function to capture or reset counter value
- Watchdog Timer
  - Supports multiple clock sources
    - CPU clock divided by 2048
    - 10 kHz internal low-speed RC oscillator (default)
    - 32.768 kHz internal low-speed external crystal oscillator
  - 8 selectable time-out periods from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - Supports multiple clock sources
    - CPU clock divided by 2048 (default)
    - 10 kHz Internal low-speed RC oscillator
  - Window set by 6-bit counter with 11-bit pre-scale
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on time-out
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
  - Supports 96 bytes backup registers
  - Programmable backup-register erase function
  - Supports external power input pin (V_{Bat})
  - Supports tamper detection function

- PWM x2
  - Supports up to two 6-channel PWM outputs with 16-bit resolution
  - Supports 8-bit presale and clock divider
  - Supports period-point, center-point and edge-point PWM Interrupts
  - Supports One-shot or Auto-reload PWM counter operation mode
  - Supports Edge-aligned or Center-aligned PWM counter type
  - Supports 8-bit dead zone with maximum divided 8 pre-scale
  - Supports brake function source from external pin or comparator outputs
  - Supports mask function for each PWM pin
  - Supports independent, complementary, synchronized and group PWM output mode
  - Supports trigger ADC start conversion at PWM counter period point, PWM counter center point, PWM output rising edge and PWM output falling edge
  - Supports 12 Capture input channels with 16-bit resolution
  - Supports rising or falling capture condition
  - Supports capture interrupt
- EPWM (Enhanced PWM) x2
  - Supports up to two EPWM
  - Each EPWM has
    - Three independent 16-bit PWM duty control units with maximum 6 port pins:
      - Three independent PWM output: PWM00, PWM02 and PWM04 for Unit 0 PWM10, PWM12 and PWM14 for Unit 1
      - Three complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion: (PWM*x*0,PWM*x*1), (PWM*x*2,PWM*x*3) and (PWM*x*4,PWM*x*5) where *x*=0~1.
      - Three synchronous PWM pairs, with each pin in a pair in-phase: (PWM0,PWM1), (PWM2,PWM3) and (PWM4,PWM5)
    - Group control bit: PWM2 and PWM4 are synchronized with PWM0
    - Supports Edge-aligned mode and Center-aligned mode
    - Programmable dead-time insertion between complementary paired PWMs
    - Each pin of from PWM0 to PWM5 has independent polarity setting control
    - Mask output control for Electrically Commutated Motor operation
    - Tri-state output at reset and brake state
    - Hardware brake protections.
    - Two Interrupt Sources:
      - Interrupt is synchronously requested at PWM frequency when up/down counter comparison matched (Edge- and Center-aligned modes) or underflow (Center-aligned mode).
      - Interrupt is requested when external brake pins asserted
    - PWM signals before polarity control stage are defined in view of positive logic. The PWM ports active high or active low are controlled by polarity control register.
    - High Source/Sink current
- Quadrature Encoder Interface (QEI) x2
  - Supports up to two QEI controllers, QEI0 and QEI1
  - Two QEI phase inputs, QEA and QEB; One Index input.
  - Each QEI has
    - Two QEI phase inputs, QEA and QEB; One Index input.
    - One QEI control register (QEI_CTR) and one QEI Status Register (QEI_STS)
    - Four Quadrature encoder pulse counter operation modes
      - Mode0: x4 free-counting mode
      - Mode1: x2 free-counting mode

- Mode2: x4 compare-counting mode
- Mode3: x2 compare-counting mode
- Encoder Pulse Width measurement mode

- Enhanced Input Capture Timer x2
  - Supports up to two Input Capture Timer/Counter Units, Input Capture 0 and Input Capture 1.
  - Each unit has own interrupt vector
  - Each unit has own interrupt vector
  - 24-bit Input Capture up-counting timer/counter
  - With noise filter in front end of input ports
  - Edge detector with three options
    - Rising edge detection
    - Falling edge detection
    - Both edge detection
  - Each input channel is supported with one capture counter hold register
  - Captured event reset/reload capture counter option
  - Supports compare-match function.
- UART x6
  - Supports up to six UART controllers
  - Supports flow control (CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1~5 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control.
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode
  - Supports Smart Card function
- Smart Card Interface x6
  - Supports up to six ISO-7816-3 ports
  - Compliant to ISO-7816-3 T=0, T=1
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - A 24-bit and two 8 bit time out counter for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports stop clock level and clock stop (clock keep) function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation/deactivation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART function
  - Supports PDMA mode
- SPI x4
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Supports 2-bit Transfer mode
  - Supports Dual and Quad I/O Transfer mode
  - Configurable bit length of a transfer word from 8 to 32-bit
  - Provides separate 8-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence

- Supports byte reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Master up to 32 MHz, and Slave up to 16 MHz (at 5V)

- I^2C x5
  - Supports up to five sets of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports speed up to 1 Mbps
  - Supports PDMA mode
  - Supports multi-address wake-up function
- I^2S x2
  - Supports up to two I^2S interface
  - Interface with external audio CODEC
  - Supports Master and Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Each provides two 8-word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Each supports two PDMA requests, one for transmitting and the other for receiving
- CAN 2.0 x2
  - Supports up to two CAN controllers
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - Each supports 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Supports interrupts
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Supports power-down wake-up function
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Controller
  - Supports one set of USB 2.0 FS Device/Host/OTG or USB 2.0 HS Device
  - Supports one set of USB 2.0 FS Host
  - FS Host compatible with Open HCI 1.0 specification

- Compliant to USB specification version 2.0
- OTG compliant with USB OTG Supplement 1.3
- On-chip USB Transceiver
- Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provides 12 programmable endpoints and one dedicated control end point
- Supports 4095 Bytes internal SRAM as USB buffer
- Provides remote wake-up capability
- On-chip 5V to 3.3V LDO for USB PHY
- On-chip PLL able to support 480 MHz clock
- Supports DMA master

- EBI
  - Supports accessible space up to 256 MB configured into 4 memory blocks (64 MB/Memory Block) , the actually external addressable space is dependent on package pin out
  - Dedicated external chip select pin for each memory block
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
  - Supports PDMA mode
  - Supports Address/Data Separated/Multiplexed Mode
  - Supports Timing parameters individual adjustment for each memory block
  - Supports “Timing Transparent Encrypt/Decrypt” for protecting data in each memory block (Individual Enable/Disable)
- Image Sensor Interface
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 3M pixel
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data format supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
  - Vertical and horizontal scaling-down for preview mode supported
  - Scaling factor as N/M
  - Two pairs of configurable 8-bit N and 8-bit M for vertical and horizontal scaling-down
  - The value of N has to be equal to or less than M
  - Frame rate control supported
  - Combines two interlace fields to a single frame supported for data in from TV-decoder
- ADC x2
  - Supports two operating modes: ADC mode and EADC (Enhance ADC mode with dual ADC Sampling)
  - Selected as ADC mode
    - Supports single 12-bit ADC conversion
    - Analog input voltage range: 0~Vref (Max to AVDD)
    - 12-bit resolution and 10-bit accuracy is guaranteed
    - Up to 800 KSPS conversion rate at 3.3V, 1 MSPS at 5V
    - Up to 12 external single-ended analog input channels
    - Up to 6 differential analog input pairs
    - Supports single ADC interrupt
    - Supports easy control for power saving
    - External V_{ref} pin can be used as input
    - Supports PDMA transfer
  - Selected as EADC mode
    - Supports two 12-bit ADC simultaneous conversion

- Analog input voltage range: 0~V_{ref} (Max to AVDD)
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 external single-ended analog input channels
- Each ADC can convert individually at normal operation
- Four ADC interrupts with individual interrupt vector addresses
- Up to 1.6M SPS conversion rate, each of ADC converter conversion time is less than 1.25μs
- An A/D conversion source can be triggered by:
  - Software trigger
  - External pin trigger
  - Timer0~3 overflow pulse triggers
  - End of conversion (EOC) pulse triggers
  - PWM triggers
- Conversion results are held in 16 data registers with valid and overrun indicators
- Sampling-oriented trigger setting and input setting for each sampling
  - Individual trigger source setting
  - Individual channel select setting
  - Individual data registers hold conversion result for each sampling setting
- Supports converting internal OP0,OP1 Amplifier output voltage
- Supports converting internal band-gap voltage, internal temperature sensor output and analog ground

- Analog Comparator x3
  - Supports up to three rail-to-rail analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupts generated when compare results change
  - Supports power-down wake-up
- Operational Amplifier x2
  - Supports up to two analog operational amplifiers
  - Outputs can be used as the input of ADC
- Cryptographic Accelerator
  - DES/TDES accelerator
    - Supports hardware DES (Data Encryption Standard)/TDES (Triple DES) accelerator
    - Supports 56, 112 and 168-bit keys
    - Supports ECB, CBC, CFB, OFB and CTR modes
    - Compliant with NIST 800 38A
  - AES accelerator
    - Supports hardware AES (Advanced Encryption Standard) accelerator
    - Supports 128-, 192- and 256-bit keys
    - Supports ECB, CBC, CFB, OFB and CTR modes
    - Compliant with NIST 800 38A
  - Secure Hash Function accelerator
    - Supports hardware SHA (Secure Hash) accelerator
    - Supports SHA-1 and SHA-224, -256
    - Compliant with FIPS 180-2
- Random Number Generator
  - Supports true random bit generator
  - Supports a random number generator programmable 64, 128, 192 and 256 bits
- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.

- Supports 8/16/32-bit of data width
- Interrupt generated once checksum error occurs

- SD Host Interface
  - Supports SD (Secure Digital) card and SD Host interface
  - Compliant with SD Memory Card Specification Version 2.0
  - Compliant with SD IO Card Specification Version 2.0
  - Supports 1 and 4-bit modes
  - Supports 25 MHz to achieve 100 Mbps at 3.3V operation
  - Supports DMA master
- Tamper Detection
  - Supports external tamper detection up to 2 input pins
  - Reset, NMI or Interrupt generated once tamper detected
- Debug
  - Supports Flash Patch and Breakpoint Unit (FPB)
    - Supports 8 hardware breakpoints
    - Supports 6 watchpoints
  - Supports the following debug ports:
    - 2-pin Serial Wire Debug port (SWD)
    - Serial Wire Viewer (SWV)
- Supports 128-bit Unique ID (UID) for security
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/ 3.8 V/ 2.7 V/ 2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40℃~105℃
- Packages
  - All Green package (RoHS)
  - LQFP 144-pin/ 128-pin/ 100-pin/ 100-pin
  -

3 PARTS INFORMATION LIST

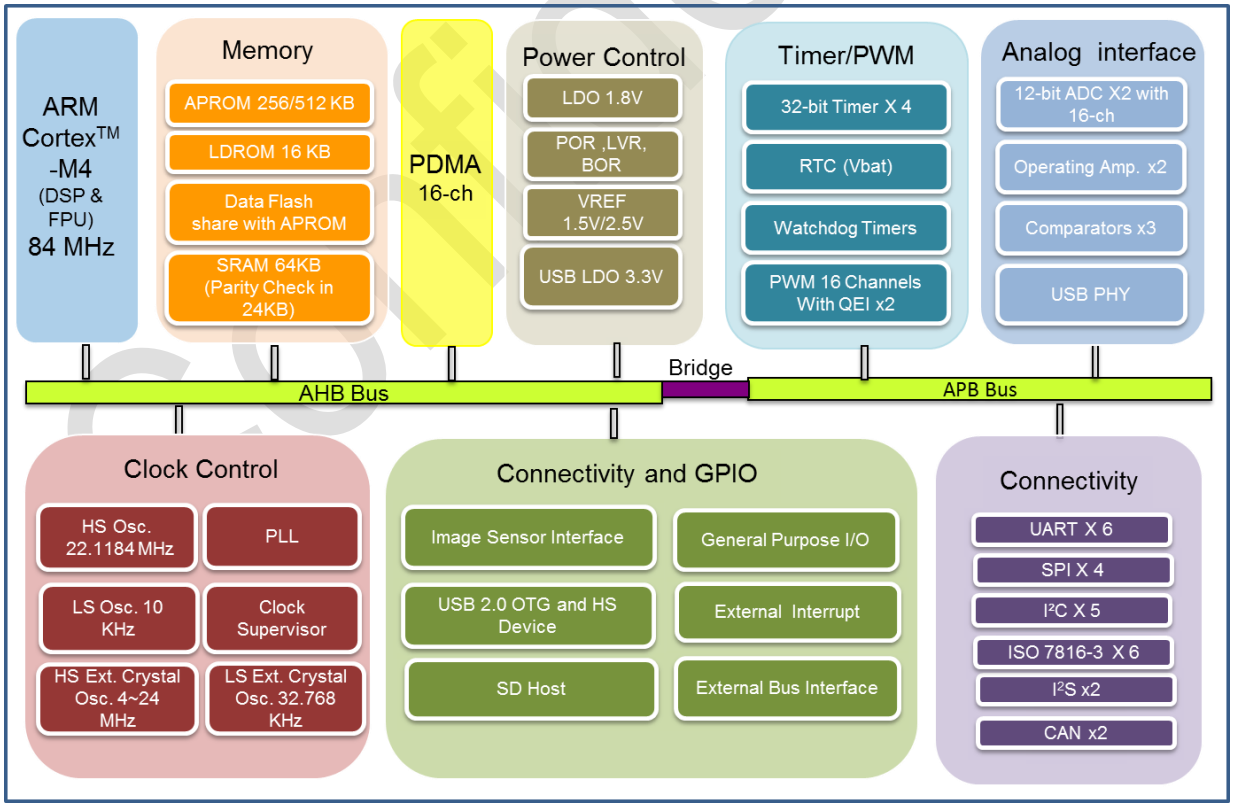
3.1 NuMicro™ NUC440xxxAE Selection Guide

3.1.1 NuMicro™ NUC440 Connectivity Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	I/O	Timer	Connectivity								Ether-net	PWM	Comp	OP	12-bit ADC	RTC	ISP ICP IAP	Pack-age
						UART	SPI	I²C	USB	LIN	CAN	SC	I²S								
NUC442JI8AE	512	64	16	114	4	6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	v	LQFP 144
NUC442JG8AE	256	64	16	114	4	6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	v	LQFP 144
NUC442KI8AE	512	64	16	100	4	6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	v	LQFP 128
NUC442KG7AE	256	64	16	100	4	6	4	5	v	6	2	6	2	--	16	3	2	x2, 16-ch	v	v	LQFP 128
NUC442VI8AE	512	64	16	77	4	6	4	5	v	6	2	6	2	--	16	3	--	x2, 16-ch	v	v	LQFP 100
NUC442VG7AE	256	64	16	77	4	6	4	5	v	6	2	6	2	--	16	3	--	x2, 16-ch	v	v	LQFP 100
NUC442RI8AE	512	64	16	45	4	4	3	2	v	4	2	3	1	--	8	2	--	x2, 8-ch	v	v	LQFP 64
NUC442RG7AE	256	64	16	45	4	4	3	2	v	4	2	3	1	--	8	2	--	x2, 8-ch	v	v	LQFP 64

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC440 Block Diagram



Important Notice

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Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.