ARM Cortex® -M0

32-bit Microcontroller

NuMicro® Family
NM1230 Series
Data Brief

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1 GENERAL DESCRIPTION

The NuMicro® NM1230 series 32-bit microcontrollers are embedded with ARM® Cortex®-M0 core for industrial applications which need high performance, high integration, and low cost. The Cortex®-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NM1230 series can run up to 48(72) MHz and operate at 2.2V(3.3V) ~ 5.5V, -40℃ ~ 105℃, and thus can support a variety of industrial control applications which need high CPU performance. The NM1230 offers 64 Kbytes embedded program Flash, size configurable Data Flash (shared with program flash), 7.5 Kbytes Flash for the ISP, 1.5 Kbytes SPROM for security, and 16Kbytes SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I²C, PWM, ADC, OP, PGA, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM1230 to reduce component count, board space and system cost. These useful functions make the NM1230 powerful for a wide range of applications.

Additionally, the NM1230 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 48/72 MHz by internal RC oscillator optioned from ROMMAP
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Built-in LDO for wide operating voltage ranged: 2.2 V to 5.5 V
- Memory
  - 64 Kbytes Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 7.5 KB Flash memory for loader (LDROM)
  - Three 0.5 KB Flash memory for security protection (SPROM0, 1, 2)
  - 16 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz external crystal input (HXT)
  - 32.768 kHz external crystal input (LXT) for idle wake-up and system operation clock
  - 48(72) MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
  - 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up
- I/O Port
  - Up to 44 general-purpose I/O (GPIO) pads and 1 Reset pad
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional TTL/Schmitt trigger input
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - GPIO built-in Pull-up/Pull-low resistor for selection.
- Timer

- Provides four channel 32-bit Timers; one 8-bit pre-scalar counter with 24-bit up-timer for each timer
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous operation modes
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
- Supports event counter function
- Supports Toggle Output mode
- Supports wake-up from Idle or Power-down mode

- Continuous Capture
  - Timer0, Timer1, Timer2, Timer3 and Systick provided with continuous capture function to capture at most 4 edges continuously on one signal
- ECAP (Enhanced Input Capture)
  - One units of 24-bit input capture counter
  - Capture surce:
    - I/O inputs: ECAP ports(ECAP0, ECAP1 and ECAP2)
    - ACMP Trigger
    - ADC Trigger
- QEI (Quadrature Encoder Interface)
  - One unit of Quadrature Encoder Interface with 3 inputs QEI_A, QEI_B and IDX
- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- EPWM
  - Supports a built-in 16-bit PWM clock generators, providing SIX PWM outputs or three complementary paired PWM outputs
  - Shared same as clock source, clock divider, period and dead-zone generator
  - Supports group/independent/complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Supports Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake and software brake protections
  - Support three of hardware Brake pin
  - Supports rising, falling, central, period, and fault break interrupts

- Supports duty/period trigger A/D conversion
- Timer comparing matching event trigger PWM to do phase change
- Supports comparator event trigger PWM to force PWM output low for current period
- Provides interrupt accumulation function

- BPWM
  - One 16-bit PWM generator which supports one 8-bit pre-scalar, one clock divider, two PWM timers (down counter) and one dead-zone generator
  - Two independent outputs or one complementary paired outputs.
  - PWM Interrupt request synchronized with PWM period
  - Edge-aligned type or Center-aligned type option
- USCI (Universal Serial Control Interface Controller)
  - Three USCI devices
  - USCI0 & USCI1 Supports to be configured as UART, SPI or I²C individually
  - USCI2 Supports to be configured as UART and I²C individually
  - Supports programmable baud-rate generator
- ADC (Analog-to-Digital Converter)
  - 12-bit ADC with 1us conversion time
  - Supports 2 sample/hold
  - Up to 16-ch single-end input from I/O and one internal input from band-gap.
  - Conversion started either by software trigger, PWM trigger, ACMP trigger or external pin trigger
  - Supports temperature sensor for measurement chip temperature
  - Supports Simultaneous and Sequential function to continuous conversion 4 channels maximum.
- Programmable Gain Amplifier (PGA)
  - Supports 8 level gain selects from 1, 2, 3, 5, 7, 9, 11 and 13.
  - Unity gain frequency up to 6 MHz
- OP Amplifier
  - Rail-to-rail OPA x 3
- DAC
  - Built-in two of 12-bit DAC,
  - Be the reference voltage for ACMP, PGA, ADC or output to pins.
- Analog Comparator
  - Two analog comparators with 4 reference voltage source
    - Programmable 16-level resistor ladders (CRV)
    - Built-in 12-bit DAC for comparator reference voltage

  - Band-gap voltage
  - External voltage from port pin
- Supports Hysteresis function 0/20/90/150mV at V_{DD} = 5V
- Interrupt when compared results changed

- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
  - Support 3 group of independent dividend, divisor, quotient and remainder registers for three times of calculation capacity
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - 8 programmable threshold levels: 4.3V/4.0V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP(7x7mm), 48-pin QFN(7x7mm)

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
DAC	Digital -to-Analog Converter
DAP	Debug Access Port
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	48 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
ISR	Interrupt Service Routine
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LXT	32.768 kHz External Low Speed Crystal Oscillator
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Selection Guide

4.1.1 NuMicro® NM1230 Series Selection Guide

Note: LQFP48: 7x7mm, QFN48: 7x7mm

Part Number	Flash (KB)	SRAM (KB)	ISP Loader ROM (KB)	Data Flash	I/O	Timer	Connectivity			IRC 48/72 MHz	PWM	BPWM	Analog Comp.	PGA	OPA	ADC (12-bit)	DAC (12-bit)	Temperature Sensor	ICP/ISPI/AP	Package
							USCI													
							UART	I²C	SPI											
NM1234D	64	16	7.5	√	44	4	3	3	2	1	6	2	2	1	3	16	2[a]	1	√	LQFP48
NM1234Y	64	16	7.5	√	44	4	3	3	2	1	6	2	2	1	3	16	2[a]	1	√	QFN48

Table 4.1-1 NuMicro® NM1230 Base Series Selection Guide

Note:

a. DAC0 outputs through PGAO by software configuration.

4.2 Pin Configuration

4.2.1 NuMicro® NM1230 Series LQFP48 (7x7mm) Pin Diagram

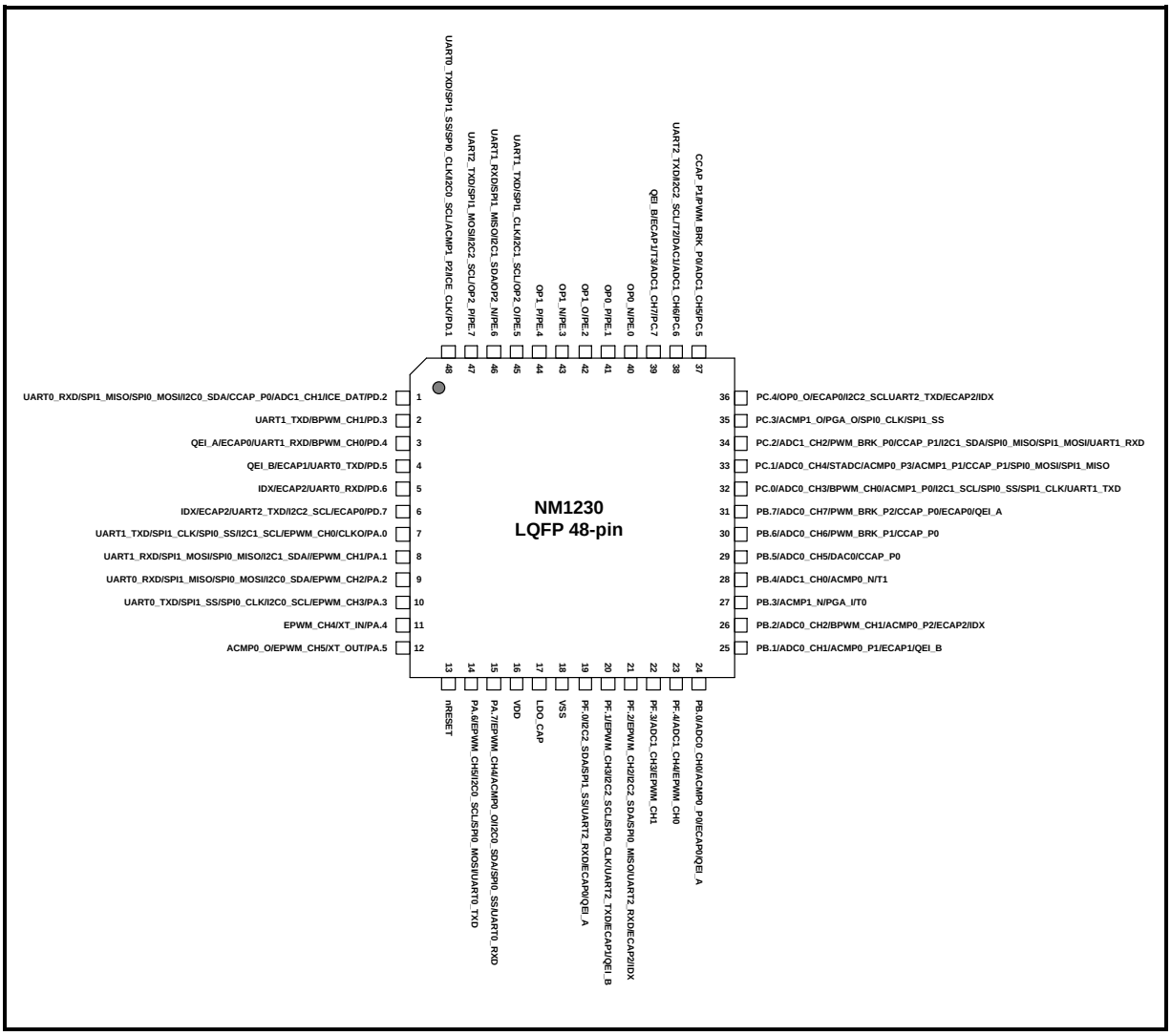


Figure 4.2-1 NuMicro® NM1230 Base Series LQFP 48-pin Diagram

4.2.2 NuMicro® NM1230 Series QFN48 (7x7mm) Pin Diagram

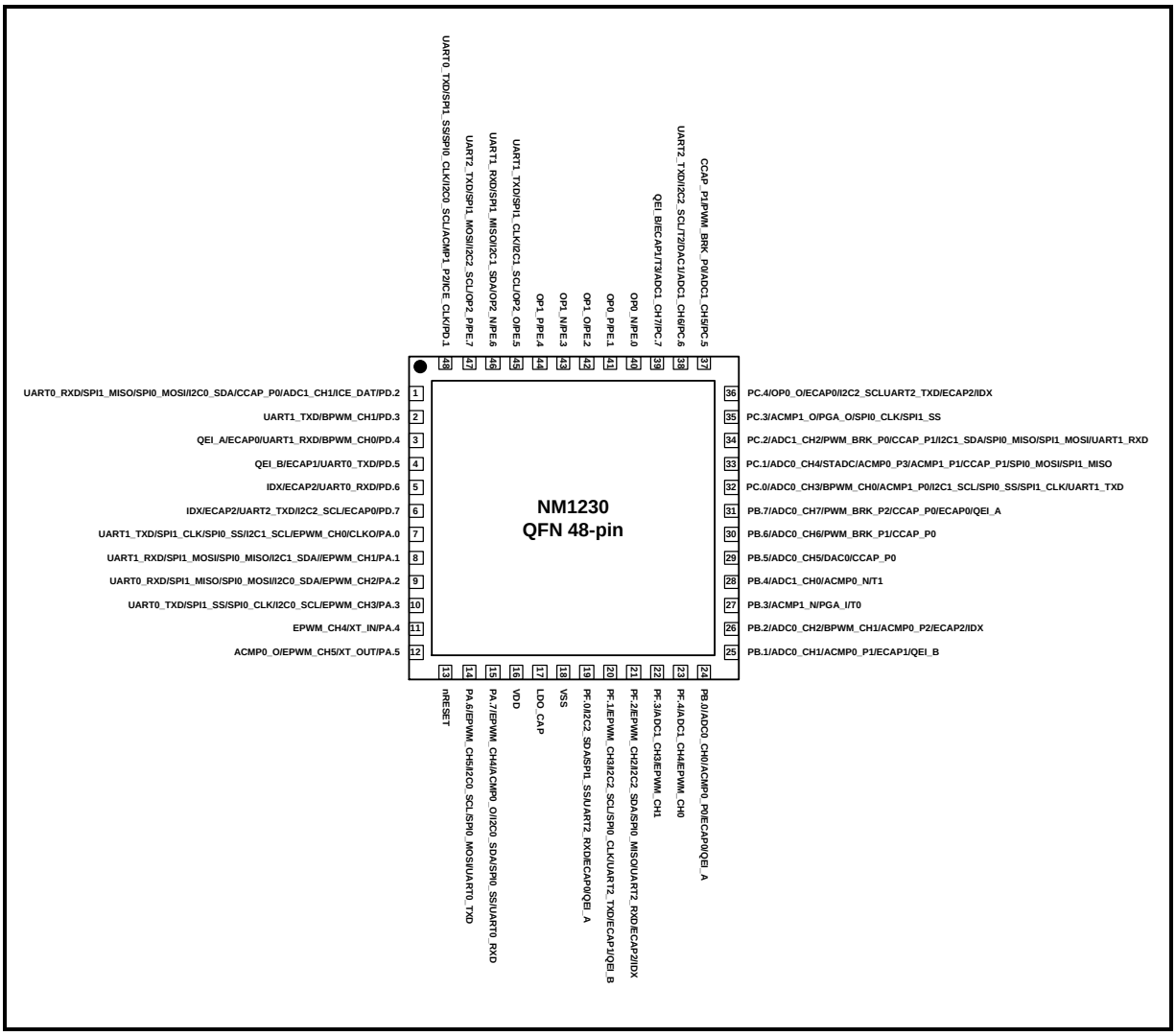


Figure 4.2-2 NuMicro® NM1230 Base Series QFN 48-pin Diagram

4.3 Pin Description

4.3.1 NM1230 Series Pin Description Overview

GPIO MFP0	ICE XTAL MFP1		ADC MFP2		PWM MFP3		ACMP0 MFP4		ACMP1 MFP5		PGA(OP) MFP6		TIMER MFP7		I2C MFP8		SPI0 MFP9		SPI1 MFPA		UART MFPB		ECAP MFPC		QEI MFPD	
GPA0	CLKO	O			EPWM_CH0	O									I²C1_SCL	IO	SPI0_SS	IO	SPI1_CLK	IO	UART1_TXD	O				
GPA1					EPWM_CH1	O									I²C1_SDA	IO	SPI0_MISO	IO	SPI1_MOSI	IO	UART1_RXD	I				
GPA2					EPWM_CH2	O									I²C0_SDA	IO	SPI0_MOSI	IO	SPI1_MISO	IO	UART0_RXD	I				
GPA3					EPWM_CH3	O									I²C0_SCL	IO	SPI0_CLK	IO	SPI1_SS	IO	UART0_TXD	O				
GPA4	XT_IN	A			EPWM_CH4	O																				
GPA5	XT_OUT	A			EPWM_CH5	O	ACMP0_O	O																		
GPA6					EPWM_CH5	O									I²C0_SCL	IO	SPI0_MOSI	IO			UART0_TXD	IO				
GPA7					EPWM_CH4	O	ACMP0_O	O							I²C0_SDA	IO	SPI0_SS	IO			UART0_RXD	IO				
GPB0			ADC0_CH0	A			ACMP0_P0	A					ECAP0	I									ECAP0	I	QEI_A	I
GPB1			ADC0_CH1	A			ACMP0_P1	A					ECAP1	I									ECAP1	I	QEI_B	I
GPB2			ADC0_CH2	A	BPWM_CH1	O	ACMP0_P2	A					ECAP2	I									ECAP2	I	IDX	I
GPB3									ACMP1_N	A	PGA_I	A	T0	IO												
GPB4			ADC1_CH0	A			ACMP0_N	A					T1	IO												
GPB5			ADC0_CH5	A			DAC0	A					CCAP_P0	I												
GPB6			ADC0_CH6	A	PWM_BRK_P1	I							CCAP_P0	I												
GPB7			ADC0_CH7	A	PWM_BRK_P2	I							CCAP_P0	I									ECAP0	I	QEI_A	I
GPC0			ADC0_CH3	A	BPWM_CH0	O			ACMP1_P0	A					I²C1_SCL	IO	SPI0_SS	IO	SPI1_CLK	IO	UART1_TXD	O				
GPC1			ADC0_CH4	A	STADC	I	ACMP0_P3	A	ACMP1_P1	A			CCAP_P1	I			SPI0_MOSI	IO	SPI1_MISO	IO						
GPC2			ADC1_CH2	A	PWM_BRK_P0	I							CCAP_P1	I	I²C1_SDA	IO	SPI0_MISO	IO	SPI1_MOSI	IO	UART1_RXD	I				
GPC3									ACMP1_O	O	PGA_O	A					SPI0_CLK	IO	SPI1_SS	IO						
GPC4											OP0_O	A	ECAP0	I	I²C2_SCL	IO					UART2_TXD	IO	ECAP2	I	IDX	I
GPC5			ADC1_CH5	A	PWM_BRK_P0	I							CCAP_P1	I												
GPC6			ADC1_CH6	A					DAC1	A			T2	IO	I²C2_SCL	IO					UART2_TXD	IO				
GPC7			ADC1_CH7	A									T3	IO									ECAP1	I	QEI_B	I
nRESET																										
GPD1	ICE_CLK	I							ACMP1_P2	A					I²C0_SCL	IO	SPI0_CLK	IO	SPI1_SS	IO	UART0_TXD	O				
GPD2	ICE_DAT	IO	ADC1_CH1	A									CCAP_P0	I	I²C0_SDA	IO	SPI0_MOSI	IO	SPI1_MISO	IO	UART0_RXD	I				
GPD3					BPWM_CH1	O															UART1_TXD	O				
GPD4					BPWM_CH0	O															UART1_RXD	I	ECAP0	I	QEI_A	I
GPD5																					UART0_TXD	IO	ECAP1	I	QEI_B	I
GPD6																					UART0_RXD	IO	ECAP2	I	IDX	I
GPD7													ECAP0	I	I²C2_SCL	IO					UART2_TXD	IO	ECAP2	I	IDX	I
GPE0											OP0_N	A														
GPE1											OP0_P	A														
GPE2											OP1_O	A														
GPE3											OP1_N	A														
GPE4											OP1_P	A														
GPE5											OP2_O	A			I²C1_SCL	IO			SPI1_CLK	IO	UART1_TXD	O				
GPE6											OP2_N	A			I²C1_SDA	IO			SPI1_MISO	IO	UART1_RXD	I				
GPE7											OP2_P	A			I²C2_SCL	IO			SPI1_MOSI	IO	UART2_TXD	IO				
GPF0															I²C2_SDA	IO			SPI1_SS	IO	UART2_RXD	IO	ECAP0	I	QEI_A	I
GPF1					EPWM_CH3	O									I²C2_SCL	IO	SPI0_CLK	IO			UART2_TXD	IO	ECAP1	I	QEI_B	I
GPF2					EPWM_CH2	O									I²C2_SDA	IO	SPI0_MISO	IO			UART2_RXD	IO	ECAP2	I	IDX	I
GPF3			ADC1_CH3	A	EPWM_CH1	O																				
GPF4			ADC1_CH4	A	EPWM_CH0	O																				

4.3.2 NM1230 Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

MFP only configures the ouput data or input data of PAD, the direction of PAD were configured by PMD.

The priority of MFP in the same multi-function was GPA > GPB > GPC > GPD > GPE > GPF.

The type A of multi-function needs to be configured to be input port.

4.3.2.1 NM1230 Series LQFP48/QFN48 Pin Description

Pin No.	Pin Name	Type	MFP*	Description
1	PD.2	I/O	MFP0	General purpose digital I/O pin.
	ICE_DAT	I/O	MFP1	Serial wired debugger data pin
	ADC1_CH1	A	MFP2	ADC1 channel analog input.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
2	PD.3	I/O	MFP0	General purpose digital I/O pin.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
3	PD.4	I/O	MFP0	General purpose digital I/O pin.
	BPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
	ECAP0	I	MFPC	Enhanced Input Capture input pin
	QEI_A	I	MFPD	Quadrature Encoder input pin
4	PD.5	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
	ECAP1	I	MFPC	Enhanced Input Capture input pin
	QEI_B	I	MFPD	Quadrature Encoder input pin
5	PD.6	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
	ECAP2	I	MFPC	Enhanced Input Capture input pin
	IDX	I	MFPD	Quadrature Encoder input pin
6	PD.7	I/O	MFP0	General purpose digital I/O pin.

Pin No.	Pin Name	Type	MFP*	Description
	ECAP_P0	I	MFP7	Enhanced Input Capture input pin
	I2C2_SCL	I/O	MFP8	I²C2 clock pin.
	UART2_TXD	O	MFPB	Data transmitter output pin for UART0.
	ECAP2	I	MFPC	Enhanced Input Capture input pin
	IDX	I	MFPD	Quadrature Encoder input pin
7	PA.0	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP1	Clock Out
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
	I2C1_SCL	I/O	MFP8	I²C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
8	PA.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	I2C1_SDA	I/O	MFP8	I²C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
9	PA.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C0_SDA	I/O	MFP8	I²C0 data input/output pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
10	PA.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C0_SCL	I/O	MFP8	I²C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
11	PA.4	I/O	MFP0	General purpose digital I/O pin.
	XT_IN	I	MFP1	External 4~24 MHz (high speed) crystal input pin.
	EPWM_CH4	I/O	MFP3	PWM channel4 output/capture input.

Pin No.	Pin Name	Type	MFP*	Description
12	PA.5	I/O	MFP0	General purpose digital I/O pin.
	XT_OUT	O	MFP1	External 4~24 MHz (high speed) crystal output pin.
	EPWM_CH5	I/O	MFP3	PWM channel5 output/capture input.
	ACMP0_O	O	MFP4	Analog comparator0 output.
13	nRESET	I		External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
14	PA.6	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH5	I/O	MFP3	PWM channel5 output/capture input.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.
15	PA.7	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH4	I/O	MFP3	PWM channel5 output/capture input.
	ACMP0_O	O	MFP4	Analog comparator0 output.
	I2C0_SDA	I/O	MFP8	I^2C0 data input/output pin.
	SPI0_SS	I/O	MFP9	SPI0 slave select pin
	UART0_RXD	I	MFPB	Data receiver input pin for UART0.
16	V_{DD}	PWR	--	Ground pin for digital circuit.
17	LDO_CAP	A	--	LDO output pin. **Note:** Recommend to connect a 1uF CAP to the pin.
18	V_{SS}	PWR	--	Ground pin for digital circuit.
19	PF.0	I/O	MFP0	General purpose digital I/O pin.
	I2C2_SDA	I/O	MFP8	I^2C2 data input/output pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART2_RXD	I	MFPB	Data receiver input pin for UART2.
	ECAP0	I	MFPC	Enhanced Input Capture input pin
	QEI_A	I	MFPD	Quadrature Encoder input pin
20	PF.1	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
	I2C2_SCL	I/O	MFP8	I^2C2 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	UART2_TXD	O	MFPB	Data transmitter output pin for UART2.
	ECAP1	I	MFPC	Enhanced Input Capture input pin
	QEI_B	I	MFPD	Quadrature Encoder input pin

Pin No.	Pin Name	Type	MFP*	Description
21	PF.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
	I2C2_SDA	I/O	MFP8	I^2C2 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	UART2_RXD	I	MFPB	Data receiver input pin for UART2.
	ECAP2	I	MFPC	Enhanced Input Capture input pin
	IDX	I	MFPD	Quadrature Encoder input pin
22	PF.3	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH3	A	MFP2	ADC1 channel analog input.
	EPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
23	PF.4	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH4	A	MFP2	ADC1 channel analog input.
	EPWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
24	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP2	ADC0 channel analog input.
	ACMP0_P0	A	MFP4	Analog comparator0 positive input pin.
	ECAP0	I	MFP7	Enhanced Input Capture input pin
	ECAP0	I	MFPC	Enhanced Input Capture input pin
	QEI_A	I	MFPD	Quadrature Encoder input pin
25	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP2	ADC0 channel analog input.
	ACMP0_P1	A	MFP4	Analog comparator0 positive input pin.
	ECAP1	I	MFP7	Enhanced Input Capture input pin
	ECAP1	I	MFPC	Enhanced Input Capture input pin
	QEI_B	I	MFPD	Quadrature Encoder input pin
26	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP2	ADC0 channel analog input.
	BPWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
	ACMP0_P2	A	MFP4	Analog comparator0 positive input pin.
	ECAP2	I	MFP7	Enhanced Input Capture input pin
	ECAP2	I	MFPC	Enhanced Input Capture input pin
	IDX	I	MFPD	Quadrature Encoder input pin
27	PB.3	I/O	MFP0	General purpose digital I/O pin.

Pin No.	Pin Name	Type	MFP*	Description
	ACMP1_N	A	MFP5	Analog comparator1 negative input pin.
	PGA_I	A	MFP6	PGA input pin
	T0	I/O	MFP7	Timer0event counter input / toggle output
28	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH0	A	MFP2	ADC1 channel analog input.
	ACMP0_N	A	MFP4	Analog comparator0 negative input pin.
	T1	I/O	MFP7	Timer1 event counter input / toggle output
29	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH5	A	MFP2	ADC0 channel analog input.
	DAC0	A	MFP4	DAC0 analog output.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
30	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH6	A	MFP2	ADC0 channel analog input.
	PWM_BRK_P1	I	MFP3	Brake input pin of EPWM.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
31	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH7	A	MFP2	ADC0 channel analog input.
	PWM_BRK_P2	I	MFP3	Brake input pin of EPWM.
	CCAP_P0	I	MFP7	Timer Continuous Capture input pin
	ECAP0	I	MFPC	Enhanced Input Capture input pin
	QEI_A	I	MFPD	Quadrature Encoder input pin
32	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP2	ADC0 channel analog input.
	BPWM_CH0	O	MFP3	BPWM channel1 output input.
	ACMP1_P0	A	MFP5	Analog comparator1 positive input pin.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI0_SS	I/O	MFP9	SPI1 slave select pin
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
33	PC.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP2	ADC0 channel analog input.
	STADC	I	MFP3	ADC external trigger input.
	ACMP0_P3	A	MFP4	Analog comparator0 positive input pin.

Pin No.	Pin Name	Type	MFP*	Description
	ACMP1_P1	A	MFP5	Analog comparator1 positive input pin.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
	SPI0_MOSI	I/O	MFP9	SPI0 1st MOSI (Master Out, Slave In) pin.
	SPI1_MISO	I/O	MFPA	SPI1 MISO (Master In, Slave Out) pin.
34	PC.2	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH2	A	MFP2	ADC1 channel analog input.
	PWM_BRK_P0	I	MFP3	Brake input pin of EPWM.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI0_MISO	I/O	MFP9	SPI0 1st MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
35	PC.3	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_O	O	MFP5	Analog comparator1 output.
	PGA_O	A	MFP6	PGA output pin
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
36	PC.4	I/O	MFP0	General purpose digital I/O pin.
	OP0_O	A	MFP6	Operational Amplifier output pin
	ECAP0	I	MFP7	Enhanced Input Capture input pin
	I2C2_SCL	I/O	MFP8	I^2C2 clock pin.
	UART2_TXD	O	MFPB	Data transmitter output pin for UART2.
	ECAP2	I	MFPC	Enhanced Input Capture input pin
	IDX	I	MFPD	Quadrature Encoder input pin
37	PC.5	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH5	A	MFP2	ADC1 channel analog input.
	PWM_BRK_P0	I	MFP3	Brake input pin of EPWM.
	CCAP_P1	I	MFP7	Timer Continuous Capture input pin
38	PC.6	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH6	A	MFP2	ADC1 channel analog input.
	DAC1	A	MFP5	DAC1 analog output.
	T2	I/O	MFP7	Timer2 event counter input / toggle output
	I2C2_SCL	I/O	MFP8	I^2C2 clock pin.

Pin No.	Pin Name	Type	MFP*	Description
	UART2_TXD	O	MFPB	Data transmitter output pin for UART2.
39	PC.7	I/O	MFP0	General purpose digital I/O pin.
	ADC1_CH7	A	MFP2	ADC1 channel analog input.
	T3	I/O	MFP7	Timer3 event counter input / toggle output
	ECAP1	I	MFPC	Enhanced Input Capture input pin
	QEI_B	I	MFPD	Quadrature Encoder input pin
40	PE.0	I/O	MFP0	General purpose digital I/O pin.
	OP0_N	A	MFP7	Operational Amplifier Negitive input pin
41	PE.1	I/O	MFP0	General purpose digital I/O pin.
	OP0_P	A	MFP7	Operational Amplifier Positive input pin
42	PE.2	I/O	MFP0	General purpose digital I/O pin.
	OP1_O	A	MFP7	Operational Amplifier output pin
43	PE.3	I/O	MFP0	General purpose digital I/O pin.
	OP1_N	A	MFP7	Operational Amplifier Negitive input pin
44	PE.4	I/O	MFP0	General purpose digital I/O pin.
	OP1_P	A	MFP7	Operational Amplifier Positive input pin
45	PE.5	I/O	MFP0	General purpose digital I/O pin.
	OP2_O	A	MFP7	Operational Amplifier output pin
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI1_CLK	I/O	MFPA	SPI1 serial clock pin
	UART1_TXD	O	MFPB	Data transmitter output pin for UART1.
46	PE.6	I/O	MFP0	General purpose digital I/O pin.
	OP2_N	A	MFP7	Operational Amplifier Negitive input pin
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	SPI1_MISO	I/O	MFPA	SPI0 1st MISO (Master In, Slave Out) pin.
	UART1_RXD	I	MFPB	Data receiver input pin for UART1.
47	PE.7	I/O	MFP0	General purpose digital I/O pin.
	OP2_P	A	MFP7	Operational Amplifier Positive input pin
	I2C2_SCL	I/O	MFP8	I^2C1 clock pin.
	SPI1_MOSI	I/O	MFPA	SPI1 MOSI (Master Out, Slave In) pin.
	UART2_TXD	O	MFPB	Data transmitter output pin for UART2.
48	PD.1	I/O	MFP0	General purpose digital I/O pin.
	ICE_CLK	I	MFP1	Serial wired debugger clock pin

Pin No.	Pin Name	Type	MFP*	Description
	ACMP1_P2	A	MFP5	Analog comparator1 positive input pin.
	I2C0_SCL	I/O	MFP8	I^2C0 clock pin.
	SPI0_CLK	I/O	MFP9	SPI0 serial clock pin.
	SPI1_SS	I/O	MFPA	SPI1 slave select pin
	UART0_TXD	O	MFPB	Data transmitter output pin for UART0.

Table 4.3-1 LQFP48/QFN48 Pin Description

Note:

1. Do not leave the pins ICE_CLK and ICE_DAT in floating when MCU is in operatoin. User may refer to one of the following methods
    a. Add external pull-up or pull-low resistors at pins.
    b. Set the 2 pins in Quasi-mode and output high to be equivelant to internal pull high.
    c. Enable intenal pull-up by setting PD_PHEN[2:1] = 11b.
    d. Be wired to other deivce without floating at pins.

4.3.3 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFP)

PA.0 MFP0 means SYS_GPA_MFP[3:0]=0x0.

PA.4 MFP5 means SYS_GPA_MFP[19:16]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ACMP0	ACMP0_P0	PB.0	MFP4	A	Comparator0 positive input pin.
	ACMP0_P1	PB.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_P2	PB.2	MFP4	A	Comparator0 positive input pin.
	ACMP0_P3	PC.1	MFP4	A	Comparator0 positive input pin.
	ACMP0_N	PB.4	MFP4	A	Comparator0 negative input pin.
	ACMP0_O	PA.7	MFP4	O	Comparator0 output pin.
	ACMP0_O	PA.5	MFP4	O	Comparator0 output pin.
ACMP1	ACMP1_P0	PC.0	MFP5	A	Comparator1 positive input pin.
	ACMP1_P1	PC.1	MFP5	A	Comparator1 positive input pin.
	ACMP1_P2	PD.1	MFP5	A	Comparator1 positive input pin.
	ACMP1_N	PB.3	MFP5	A	Comparator1 negative input pin.
	ACMP1_O	PC.3	MPF5	O	Comparator1 output pin.
STADC	STADC	PC.1	MFP3	I	External ADC trigger input pin.
ADC0	ADC0_CH0	PB.0	MFP2	A	ADC0 analog input channel 0.
	ADC0_CH1	PB.1	MFP2	A	ADC0 analog input channel 1.
	ADC0_CH2	PB.2	MFP2	A	ADC0 analog input channel 2.
	ADC0_CH3	PC.0	MFP2	A	ADC0 analog input channel 3.
	ADC0_CH4	PC.1	MFP2	A	ADC0 analog input channel 4.
	ADC0_CH5	PB.5	MFP2	A	ADC0 analog input channel 5.
	ADC0_CH6	PB.6	MFP2	A	ADC0 analog input channel 6.
	ADC0_CH7	PB.7	MFP2	A	ADC0 analog input channel 7.
ADC1	ADC1_CH0	PB.4	MFP2	A	ADC1 analog input channel 0.
	ADC1_CH1	PD.2	MFP2	A	ADC1 analog input channel 1.
	ADC1_CH2	PC.2	MFP2	A	ADC1 analog input channel 2.
	ADC1_CH3	PF.3	MFP2	A	ADC1 analog input channel 3.
	ADC1_CH4	PF.4	MFP2	A	ADC1 analog input channel 4.
	ADC1_CH5	PC.5	MFP2	A	ADC1 analog input channel 5.
	ADC1_CH6	PC.6	MFP2	A	ADC1 analog input channel 6.
	ADC1_CH7	PC.7	MFP2	A	ADC1 analog input channel 7.
CLKO	CLKO	PA.0	MFP1	O	Clock output pin.

BPWM	BPWM_CH0	PC.0	MFP3	O	Basic PWM channel 0 output
	BPWM_CH0	PD.4	MFP3	O	Basic PWM channel 0 output
	BPWM_CH1	PB.2	MFP3	O	Basic PWM channel 1 output
	BPWM_CH1	PD.3	MFP3	O	Basic PWM channel 1 output
CCAP	CCAP_P0	PB.5	MFP7	I	Continuous Capture Input
	CCAP_P0	PB.6	MFP7	I	Continuous Capture Input
	CCAP_P0	PB.7	MFP7	I	Continuous Capture Input
	CCAP_P0	PD.2	MFP7	I	Continuous Capture Input
	CCAP_P1	PC.1	MFP7	I	Continuous Capture Input
	CCAP_P1	PC.2	MFP7	I	Continuous Capture Input
	CCAP_P1	PC.5	MFP7	I	Continuous Capture Input
ECAP	ECAP_P0	PB.0	MFP7,MFPC	I	Input capture channel 0
	ECAP_P0	PB.7	MFPC	I	Input capture channel 0
	ECAP_P0	PC.4	MFP7	I	Input capture channel 0
	ECAP_P0	PD.4	MFPC	I	Input capture channel 0
	ECAP_P0	PD.7	MFP7	I	Input capture channel 0
	ECAP_P0	PF.0	MFPC	I	Input capture channel 0
	ECAP_P1	PB.1	MFP7,MFPC	I	Input capture channel 1
	ECAP_P1	PC.7	MFPC	I	Input capture channel 1
	ECAP_P1	PD.5	MFPC	I	Input capture channel 1
	ECAP_P1	PF.1	MFPC	I	Input capture channel 1
	ECAP_P2	PB.2	MFP7,MFPC	I	Input capture channel 2
	ECAP_P2	PC.4	MFPC	I	Input capture channel 2
	ECAP_P2	PD.6	MFPC	I	Input capture channel 2
	ECAP_P2	PD.7	MFPC	I	Input capture channel 2
	ECAP_P2	PF.2	MFPC	I	Input capture channel 2
QEI	QEI_A	PB.0	MFPD	I	QEI channel input
	QEI_A	PB.7	MFPD	I	QEI channel input
	QEI_A	PD.4	MFPD	I	QEI channel input
	QEI_A	PF.0	MFPD	I	QEI channel input
	QEI_B	PB.1	MFPD	I	QEI channel input
	QEI_B	PC.7	MFPD	I	QEI channel input
	QEI_B	PD.5	MFPD	I	QEI channel input
	QEI_B	PF.1	MFPD	I	QEI channel input

	IDX	PB.2	MFPD	I	QEI channel input
	IDX	PC.4	MFPD	I	QEI channel input
	IDX	PD.6	MFPD	I	QEI channel input
	IDX	PD.7	MFPD	I	QEI channel input
	IDX	PF.2	MFPD	I	QEI channel input
EPWM	PWM_BRK_P0	PC.2	MFP3	I	EPWM brake pin.
	PWM_BRK_P0	PC.5	MFP3	I	EPWM brake pin.
	PWM_BRK_P1	PB.6	MFP3	I	EPWM brake pin.
	PWM_BRK_P2	PB.7	MFP3	I	EPWM brake pin.
	EPWM_CH5	PA.5	MFP3	O	Enhanced PWM output pin.
	EPWM_CH5	PA.6	MFP3	O	Enhanced PWM output pin.
	EPWM_CH4	PA.4	MFP3	O	Enhanced PWM output pin.
	EPWM_CH4	PA.7	MFP3	O	Enhanced PWM output pin.
	EPWM_CH3	PA.3	MFP3	O	Enhanced PWM output pin.
	EPWM_CH3	PF.1	MFP3	O	Enhanced PWM output pin.
	EPWM_CH2	PA.2	MFP3	O	Enhanced PWM output pin.
	EPWM_CH2	PF.2	MFP3	O	Enhanced PWM output pin.
	EPWM_CH1	PA.1	MFP3	O	Enhanced PWM output pin.
	EPWM_CH1	PF.3	MFP3	O	Enhanced PWM output pin.
	EPWM_CH0	PA.0	MFP3	O	Enhanced PWM output pin.
	EPWM_CH0	PF.4	MFP3	O	Enhanced PWM output pin.
nRESET	nRESET	--	--	I	External reset pin, internal pull-high.
I2C0	I2C0_SCL	PA.3	MFP8	I/O	I^2C0 clock pin.
	I2C0_SCL	PA.6	MFP8	I/O	I^2C0 clock pin.
	I2C0_SCL	PD.1	MFP8	I/O	I^2C0 clock pin.
	I2C0_SDA	PA.2	MFP8	I/O	I^2C0 data pin.
	I2C0_SDA	PA.7	MFP8	I/O	I^2C0 data pin.
	I2C0_SDA	PD.2	MFP8	I/O	I^2C0 data pin.
I2C1	I2C1_SCL	PA.0	MFP8	I/O	I^2C1 clock pin.
	I2C1_SCL	PC.0	MFP8	I/O	I^2C1 clock pin.
	I2C1_SCL	PE.5	MFP8	I/O	I^2C1 clock pin.
	I2C1_SDA	PA.1	MFP8	I/O	I^2C1 data pin.
	I2C1_SDA	PC.2	MFP8	I/O	I^2C1 data pin.
	I2C1_SDA	PE.6	MFP8	I/O	I^2C1 data pin.

I2C2	I2C2_SCL	PC.4	MFP8	I/O	I²C2 clock pin.
	I2C2_SCL	PC.6	MFP8	I/O	I²C2 clock pin.
	I2C2_SCL	PD.7	MFP8	I/O	I²C2 clock pin.
	I2C2_SCL	PE.7	MFP8	I/O	I²C2 clock pin.
	I2C2_SCL	PF.1	MFP8	I/O	I²C2 clock pin.
	I2C2_SDA	PF.0	MFP8	I/O	I²C2 data pin.
	I2C2_SDA	PF.2	MFP8	I/O	I²C2 data pin.
PGA	PGA_I	PB.3	MFP6	A	PGA analog input pin.
	PGA_O	PC.3	MFP6	A	PGA analog output pin.
DAC	DAC0	PB.5	MFP4	A	DAC0 analog output pin.
	DAC1	PC.6	MFP5	A	DAC1 analog output pin.
OP	OP0_O	PC.4	MFP6	A	OP0 analog output pin.
	OP0_N	PE.0	MFP6	A	OP0 analog input pin.
	OP0_P	PE.1	MFP6	A	OP0 analog input pin.
	OP1_O	PE.2	MFP6	A	OP1 analog output pin.
	OP1_N	PE.3	MFP6	A	OP1 analog input pin.
	OP1_P	PE.4	MFP6	A	OP1 analog input pin.
	OP2_O	PE.5	MFP6	A	OP2 analog output pin.
	OP2_N	PE.6	MFP6	A	OP2 analog input pin.
	OP2_P	PE.7	MFP6	A	OP2 analog input pin.
SPI0	SPI0_MOSI	PA.2	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MOSI	PA.6	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MOSI	PC.1	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MOSI	PD.2	MFP9	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MISO	PA.1	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MISO	PC.2	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MISO	PF.2	MFP9	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_CLK	PA.3	MFP9	I/O	SPI0 clock pin.
	SPI0_CLK	PC.3	MFP9	I/O	SPI0 clock pin.
	SPI0_CLK	PD.1	MFP9	I/O	SPI0 clock pin.
	SPI0_CLK	PF.1	MFP9	I/O	SPI0 clock pin.
	SPI0_SS	PA.0	MFP9	I	SPI0 slave selection pin.
	SPI0_SS	PA.7	MFP9	I	SPI0 slave selection pin.
	SPI0_SS	PC.0	MFP9	I	SPI0 slave selection pin.

SPI1	SPI1_MOSI	PA.1	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_MOSI	PC.2	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_MOSI	PE.7	MFPA	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_MISO	PA.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_MISO	PC.1	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_MISO	PD.2	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_MISO	PE.6	MFPA	I/O	SPI1 MISO (Master In, Slave Out) pin
	SPI1_CLK	PA.0	MFPA	I/O	SPI1 clock pin.
	SPI1_CLK	PC.0	MFPA	I/O	SPI1 clock pin.
	SPI1_CLK	PE.5	MFPA	I/O	SPI1 clock pin.
	SPI1_SS	PA.3	MFPA	I/O	SPI1 Slave Select
	SPI1_SS	PC.3	MFPA	I/O	SPI1 Slave Select
	SPI1_SS	PD.1	MFPA	I/O	SPI1 Slave Select
	SPI1_SS	PF.0	MFPA	I/O	SPI1 Slave Select
TM0	TM0	PB.3	MFP7	I	Timer0 event counter input / toggle output
TM1	TM1	PB.4	MFP7	I	Timer1 event counter input / toggle output
TM2	TM2	PC.6	MFP7	I	Timer2 event counter input / toggle output
TM3	TM3	PC.7	MFP7	I	Timer3 event counter input / toggle output
XTAL	XT_OUT	PA.5	MPF1	A	External crystal output pin.
	XT_IN	PA.4	MFP1	A	External crystal input pin.
UART0	UART0_TXD	PA.3	MFPB	O	UART0 data transmitter output pin.
	UART0_TXD	PA.6	MFPB	O	UART0 data transmitter output pin.
	UART0_TXD	PD.1	MFPB	O	UART0 data transmitter output pin.
	UART0_TXD	PD.5	MFPB	O	UART0 data transmitter output pin.
	UART0_RXD	PA.2	MFPB	I	UART0 data receiver input pin.
	UART0_RXD	PA.7	MFPB	I	UART0 data receiver input pin.
	UART0_RXD	PD.2	MFPB	I	UART0 data receiver input pin.
	UART0_RXD	PD.6	MFPB	I	UART0 data receiver input pin.
UART1	UART1_TXD	PA.0	MFPB	O	UART1 data transmitter output pin.
	UART1_TXD	PC.0	MFPB	O	UART1 data transmitter output pin.
	UART1_TXD	PD.3	MFPB	O	UART1 data transmitter output pin.
	UART1_TXD	PE.5	MFPB	O	UART1 data transmitter output pin.
	UART1_RXD	PA.1	MFPB	I	UART1 data receiver input pin.
	UART1_RXD	PC.2	MFPB	I	UART1 data receiver input pin.

	UART1_RXD	PD.4	MFPB	I	UART1 data receiver input pin.
	UART1_RXD	PE.6	MFPB	I	UART1 data receiver input pin.
UART2	UART2_TXD	PC.4	MFPB	O	UART2 data transmitter output pin.
	UART2_TXD	PC.6	MFPB	O	UART2 data transmitter output pin.
	UART2_TXD	PD.7	MFPB	O	UART2 data transmitter output pin.
	UART2_TXD	PE.7	MFPB	O	UART2 data transmitter output pin.
	UART2_TXD	PF.1	MFPB	O	UART2 data transmitter output pin.
	UART2_RXD	PF.0	MFPB	I	UART2 data receiver input pin.
	UART2_RXD	PF.2	MFPB	I	UART2 data receiver input pin.
ICE	ICE_DAT	PD.2	MFP1	I/O	Serial wired debugger data pin
	ICE_CLK	PD.1	MFP1	I	Serial wired debugger clock pin

Table 4.3-2 LQFP48 Multi-function Pin Summary

5 BLOCK DIAGRAM

5.1 NuMicro® NM1230 Block Diagram

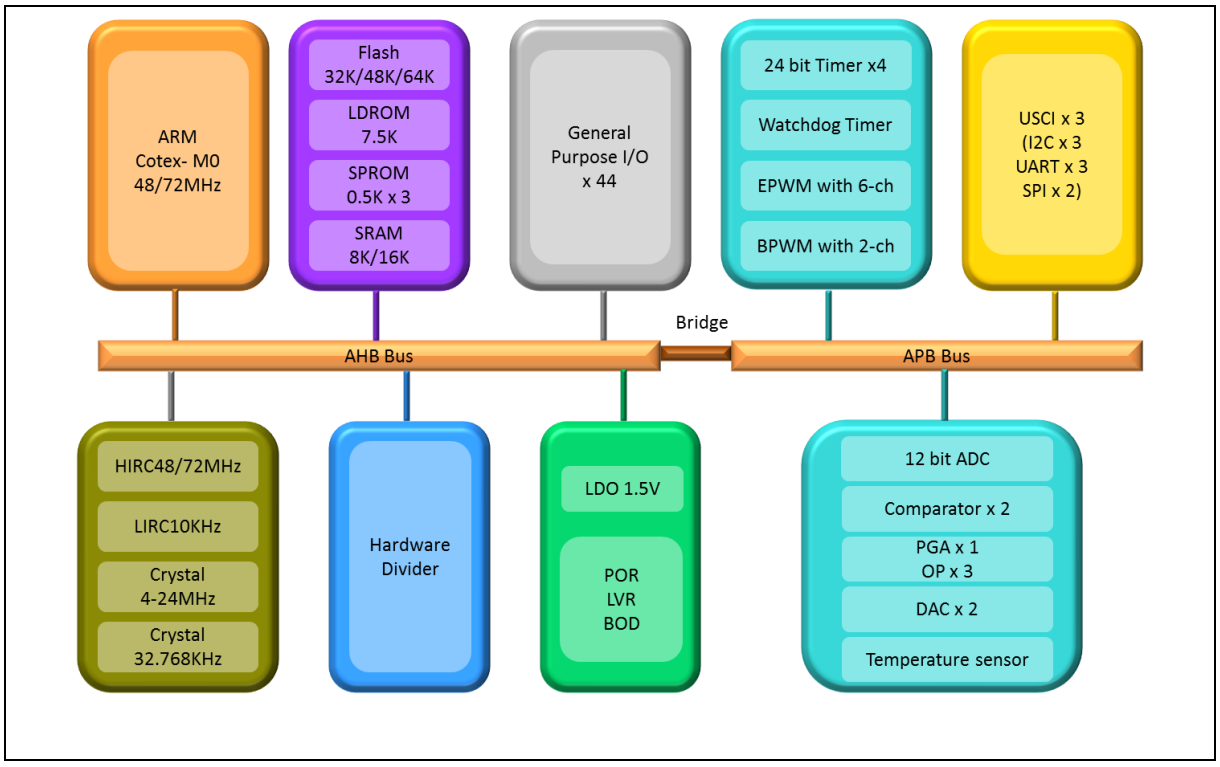


Figure 5.1-1 NuMicro® NM1230 Block Diagram

6 ELECTRICAL CHARACTERISTICS

For information on the NM1230 series electrical characteristics, please refer to NuMicro® NM1230 Series Datasheet.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} -0.3	V_{DD} +0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

6.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions			
V_{DD}	Operation voltage	2.2	-	5.5	V	V_{DD} = 2.2V ~ 5.5V up to 48 MHz V_{DD} = 3.3V ~ 5.5V up to 72 MHz			
V_{SS}	Power Ground	-0.3	-	-	V				
V_{LDO}	LDO Output Voltage		1.5		V				
V_{BG}	Band-gap Voltage[3]	1.17	1.23	1.28	V	V_{DD} = 3.0V ~ 5.5V, T_A = -40°C~105°C			
I_{DD}	Operating Current Normal Run Mode HCLK = 72 MHz while(1){} Executed from Flash	-	14.9	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	72 MHz	V
I_{DD}		-	10.3	-	mA	5.5V	X	72 MHz	X
I_{DD}		-	14.9	-	mA	3V	X	72 MHz	V
I_{DD}		-	10.3	-	mA	3V	X	72 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 48 MHz while(1){} Executed from Flash	-	10.4	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	5.5V	X	48 MHz	X
I_{DD}		-	10.4	-	mA	3V	X	48 MHz	V
I_{DD}		-	7.3	-	mA	3V	X	48 MHz	X
I_{DD}	Operating Current Normal Run Mode HCLK = 24 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	5.5V	24 MHz	X	X
I_{DD}		-	5.4	-	mA	3V	24 MHz	X	V
I_{DD}		-	4.1	-	mA	3V	24 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 16 MHz while(1){} Executed from Flash	-	3.9	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	16 MHz	X	V
I_{DD}		-	3.0	-	mA	5.5V	16 MHz	X	X
I_{DD}		-	3.9	-	mA	3V	16 MHz	X	V

I_{DD}		-	3.0	-	mA	3V	16 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	3.1	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	12 MHz	X	V
I_{DD}		-	2.5	-	mA	5.5V	12 MHz	X	X
I_{DD}		-	3.1	-	mA	3V	12 MHz	X	V
I_{DD}		-	2.4	-	mA	3V	12 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 4 MHz while(1){} Executed from Flash	-	1.5	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	4 MHz	X	V
I_{DD}		-	1.3	-	mA	5.5V	4 MHz	X	X
I_{DD}		-	1.4	-	mA	3V	4 MHz	X	V
I_{DD}		-	1.2	-	mA	3V	4 MHz	X	X
I_{DD}	Operating Current Normal Run Mode HCLK = 32 kHz while(1){} Executed from Flash	-	154	-	µA	V_{DD}	LXT	LIRC	All Digital Modules
						5.5V	32 KHz	V	V[1]
I_{DD}		-	152	-	µA	5.5V	32 KHz	V	X
I_{DD}		-	134	-	µA	3V	32 KHz	V	V[1]
I_{DD}		-	132	-	µA	3V	32 KHz	V	X
I_{DD}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	148	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	10 KHz	V[2]
I_{DD}		-	148	-	µA	5.5V	X	10 KHz	X
I_{DD}		-	128	-	µA	3V	X	10 KHz	V[2]
I_{DD}		-	128	-	µA	3V	X	10 KHz	X
I_{IDLE}	Operating Current Idle Mode HCLK= 72 MHz	-	8.3	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	3.6	-	mA	5.5V	X	V	X
I_{IDLE}		-	8.3	-	mA	3V	X	V	V

I_{IDLE}		-	3.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK= 48 MHz	-	5.7	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	X	V	V
I_{IDLE}		-	2.6	-	mA	5.5V	X	V	X
I_{IDLE}		-	5.7	-	mA	3V	X	V	V
I_{IDLE}		-	2.6	-	mA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK = 24 MHz	-	2.9	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	5.5V	24 MHz	X	X
I_{IDLE}		-	2.9	-	mA	3V	24 MHz	X	V
I_{IDLE}		-	1.6	-	mA	3V	24 MHz	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 16 MHz	-	2.2	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.3	-	mA	5.5V	V	X	X
I_{IDLE}		-	2.1	-	mA	3V	V	X	V
I_{IDLE}		-	1.3	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 12 MHz	-	1.8	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	1.1	-	mA	5.5V	V	X	X
I_{IDLE}		-	1.7	-	mA	3V	V	X	V
I_{IDLE}		-	1.1	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 4 MHz	-	1.0	-	mA	V_{DD}	HXT	HIRC	All Digital Modules
						5.5V	V	X	V
I_{IDLE}		-	0.8	-	mA	5.5V	V	X	X
I_{IDLE}		-	1.0	-	mA	3V	V	X	V

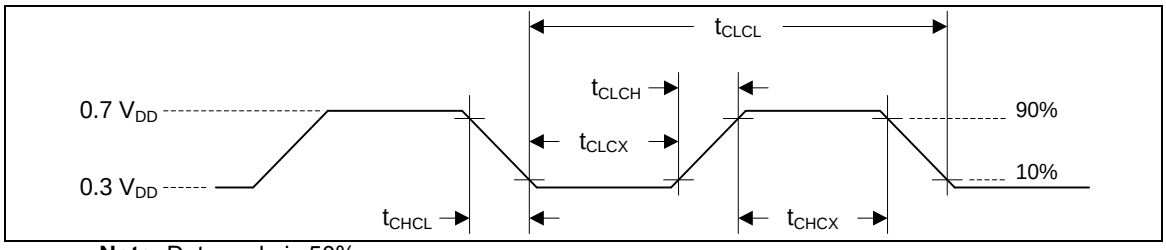
I_{IDLE}		-	0.7	-	mA	3V	V	X	X
I_{IDLE}	Operating Current Idle Mode HCLK = 32 kHz	-	150	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[1]
I_{IDLE}		-	148	-	µA	5.5V	X	V	X
I_{IDLE}		-	129	-	µA	3V	X	V	V[1]
I_{IDLE}		-	128	-	µA	3V	X	V	X
I_{IDLE}	Operating Current Idle Mode HCLK = 10 kHz	-	147	-	µA	V_{DD}	HXT	LIRC	All Digital Modules
						5.5V	X	V	V[2]
I_{IDLE}		-	147	-	µA	5.5V	X	V	X
I_{IDLE}		-	127	-	µA	3V	X	V	V[2]
I_{IDLE}		-	126	-	µA	3V	X	V	X
I_{PWD}	Standby Current Power-down Mode (Deep Sleep Mode)	-	3.6	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.			
I_{PWD}		-	2.4	-	µA	V_{DD} = 3 V, All oscillators and analog blocks turned off.			
I_{LK}	Input Leakage Current	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode			
V_{IL1}	Input Low Voltage (TTL Input)	-0.3	1.33		V	V_{DD} = 5.5 V			
		-0.3	1			V_{DD} = 3.3 V			
V_{IH1}	Input High Voltage (TTL Input)		1.47	V_{DD} + 0.3	V	V_{DD} = 5.5 V			
			1.08	V_{DD} + 0.3		V_{DD} = 3.3 V			
V_{ILS}	Negative-going Threshold (Schmitt Input), nRESET	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt Input), nRESET	$0.7V_{DD}$	-	-	V	-			
R_{UP}[3]	Internal Pull-up Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{LOW}[3]	Internal Pull-low Resistor (PA/PB/PC/PD/PE/PF)		51		kΩ	V_{DD} = 5.0V			
R_{RST}	Internal nRESET Pin Pull-up Resistor	48		148	kΩ	V_{DD} = 2.2 V ~ 5.5V			
V_{ILS}	Negative-going Threshold (Schmitt input)	-	-	$0.3V_{DD}$	V	-			
V_{IHS}	Positive-going Threshold (Schmitt input)	$0.7V_{DD}$	-	-	V	-			

I_{IL}	Logic 0 Input Current (Quasi-bidirectional Mode)	-	-63.65		μA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current	-	-566.7	-	μA	V_{DD} = 5.5 V
I_{SR}	Source Current (Quasi-bidirectional Mode)	-	-372	-	μA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR}		-	-76.8	-	μA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-37.3	-	μA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SR}	Source Current (Push-pull Mode)	-	-19.2	-	mA	V_{DD} = 4.5 V, V_{IN} = 2.4 V
I_{SR}		-	-4	-	mA	V_{DD} = 2.7 V, V_{IN} = 2.2 V
I_{SR}		-	-2	-	mA	V_{DD} = 2.2 V, V_{IN} = 1.8 V
I_{SK}	Sink Current PA/PB/PC/PD (Quasi-bidirectional, Open-Drain and Push-pull Mode)	-	12.8	-	mA	V_{DD} = 4.5 V, V_{IN} = 0.4 V
I_{SK}		-	8.1	-	mA	V_{DD} = 2.7 V, V_{IN} = 0.4 V
I_{SK13}		-	6	-	mA	V_{DD} = 2.2 V, V_{IN} = 0.4 V

Notes:
1. Only enable modules, which support 32 kHz LIRC clock source
2. Only enable modules, which support 10 kHz LIRC clock source
3. Guaranteed by design, not test in production.

6.3 AC Electrical Characteristics

6.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

6.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.2	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	414	-	uA	12 MHz, V_{DD} = 5.5V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

6.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	8~12 pF	8~12 pF

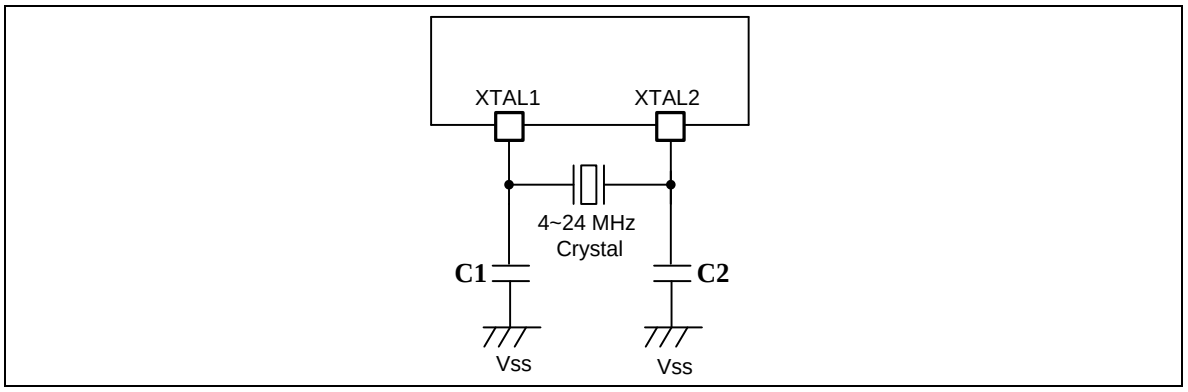


Figure 6.3-1 Typical Crystal Application Circuit

6.3.4 48/72 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	-	1.5	-	V	-
f_{HRC72}	Center Frequency	-	72	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1.5	-	+1.5	%	T_A = 25 ℃ V_{DD}=4.5 V~ 5.5 V
			2.5%		%	T_A = -40℃~105℃ V_{DD}=3.0 V~ 5.5 V
I_{HRC72}	Operating Current	-	300	-	μA	T_A = 25 ℃,V_{DD} = 5 V
f_{HRC48}	Center Frequency	-	48	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5.5 V
			2%		%	T_A = -40℃~105℃ V_{DD}=2.5 V~ 5.5 V
I_{HRC48}	Operating Current	-	280	-	μA	T_A = 25 ℃,V_{DD} = 5 V

6.3.5 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	-	1.5V	-	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-

	Oscillator Frequency	-20[1]	-	+20[1]	%	V_{DD} = 2.2 V ~ 5.5 V T_A = -40℃ ~ +105℃
I_{LRC}	Operating Current	-	0.4	-	μA	T_A = 25 ℃,V_{DD} = 5 V

Note1: These parameters are characterized but not tested.

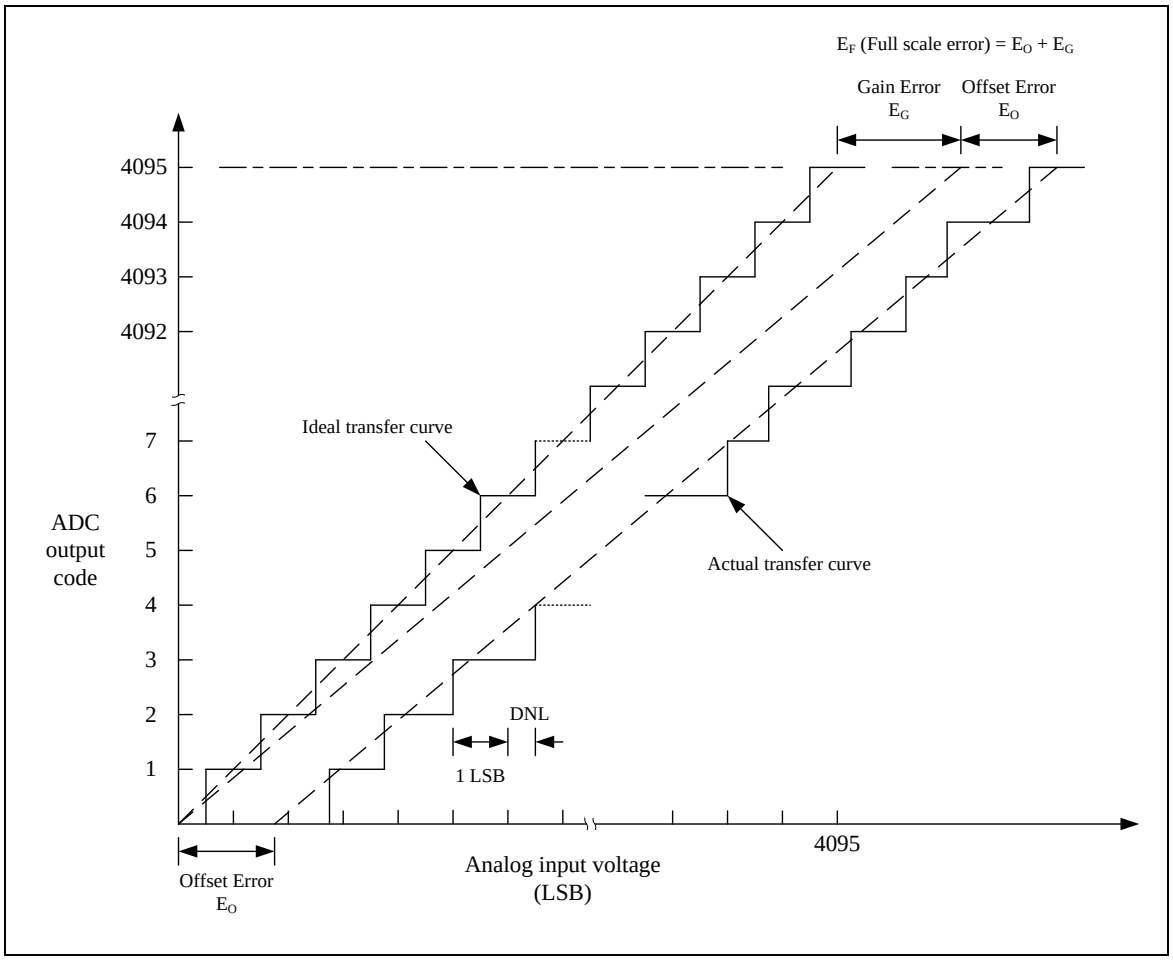
6.4 Analog Characteristics

6.4.1 12-bit SAR ADC

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	2	-	LSB	V_{DD} = 3.0 ~5.5 V
INL	Integral Nonlinearity Error	-	±2	-	LSB	V_{DD} = 3.0 ~5.5 V
E_O	Offset Error	-	±1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_G	Gain Error (Transfer Gain)	-	-1	-	LSB	V_{DD} = 3.0 ~5.5 V
E_A	Absolute Error	-	±3	-	LSB	V_{DD} = 3.0 ~5.5 V
-	Monotonic	Guaranteed			-	-
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	V_{DD} = 3.0 ~5.5 V N is sampling counter, N=1~1024
		200			ns	V_{DD} = 3.0~5.5 V
T_{CONV}	Conversion Time[3]		1000	1250	ns	V_{DD} = 3.0~5.5 V
I_{DDA}	Supply Current (Avg.)	-	1	-	mA	V_{DD} = 5.5 V
V_{IN}	Analog Input Voltage	0	-	V_{DD}	V	-
C_{IN}	Input Capacitance[2]	-	1.6	-	pF	-

1. ADC voltage reference is same with V_{DD} .
2. It's for sample and hold. The maximum value depends on process variation. Basically, the variation of C_{IN} is less than about 10% of typical value.
3. Guaranteed by design, not test in production. The conversion time is upto auto-completion of analog comparison in ADC IP and the typical value is about 1000ns at V_{DD} = 5V.


E_F (Full scale error) = E_O + E_G
Gain Error
E_G
Offset Error
E_O
4095
4094
4093
4092
7
6
5
4
3
2
1
ADC
output
code
Ideal transfer curve
Actual transfer curve
DNL
1 LSB
4095
Offset Error
E_O
Analog input voltage
(LSB)

6.4.2 LDO & Power Management

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LDO}	Output Voltage	1.35	1.5	1.65	V	-

Notes:

It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

6.4.3 Brown-out Detector

(V_{DD} – V_{SS} = 0~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{BOD}	Quiescent Current	-	40	-	μA	V_{DD} =5.5V
V_{BOH}	Brown-out Hysteresis	30	100	150	mV	
V_{BOD}	Brown-out Detector	4.15	4.3	4.45	V	BOV_VL [2:0] = 7
		3.85	4.0	4.15	V	BOV_VL [2:0] = 6
		3.55	3.7	3.85	V	BOV_VL [2:0] = 5
		2.85	3.0	3.15	V	BOV_VL [2:0] = 4
		2.55	2.7	2.85	V	BOV_VL [2:0] = 3
		2.3	2.4	2.5	V	BOV_VL [2:0] = 2
		2.1	2.2	2.3	V	BOV_VL [2:0] = 1
		1.9	2.0	2.1	V	BOV_VL [2:0] = 0

6.4.4 Power-on Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{POR}	Threshold Voltage	1.60	1.75	1.90	V	-

6.4.5 LVR Reset

(V_{DD} – V_{SS} = 0 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LVR}	Threshold Voltage	1.7	1.9	2.1	V	-

6.4.6 Comparator

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V, T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{CMP}	Operation Current	-	48		μA	V_{DD}=5.5V
V_{OFF}	Input Offset Voltage		±10		mV	-
V_{SW}	Output Swing	0	-	V_{DD}	V	-
V_{COM}	Input Common Mode Range	0.1	-	V_{DD} – 0.1	V	-
-	DC Gain[1]	-	60	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	
V_{HYS}	Hysteresis	10	20	30	mV	ACMPHYSEN = 01
V_{HYS}	Hysteresis	60	90	120	mV	ACMPHYSEN = 10
V_{HYS}	Hysteresis	95	150	200	mV	ACMPHYSEN = 11
T_{STB}	Stable time	-	1.06	-	μs	

Notes:

Guaranteed by design, not test in production.

6.4.7 PGA

(V_{DD} – V_{SS} = 2.2 ~ 5.5 V, T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Operating Current			5	mA	VDD5V=5V, T=125℃
Input Offset			+2	mV	VCM=VDD/2, T=25℃
Input Offset Average Drift			3.5	uV/℃	
Output Swing	0.1		VDD5V – 0.1	V	
PGA gain accuracy	-1		+1	%	
Input Common Mode Range	0		VDD5V- 1.5	V	
DC Gain	50	80		dB	
Unity Gain Frequency	6	7	8.2	MHz	VDD = 5V
Phase Margin	50°			°	
PSRR+	49	90		dB	VDD = 5V
CMRR	69	90		dB	VDD = 5V
Slew Rate+	6.0	-	-	V/us	VDD=5V, Rload=33K, Cload=50p
Wake Up Time			20	us	

Maximum output voltage swing from rail		40		mV	V_{DD} =5.5, RL=50K
		200		mV	V_{DD} =5.5, RL=10K

Notes:

Guaranteed by design, not test in production.

6.4.8 OP Amplifier

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Parameter	Min	Typ	Max	Unit	Test Condition
Input offset voltage	-	2	5	mV	
Input offset average drift	-	-	1	uV/℃	
Output swing	0.1	-	VDD-0.1	V	
Input common mode range	0.1	-	VDD-0.1	V	
DC gain	-	80	-	dB	
Phase margin	-	50°	-	°	
PSRR+	-	90	-	dB	VDD=5V
CMRR	-	90	-	dB	VDD=5V
Slew rate	6.0	-	-	V/us	VDD=5V, RLOAD=33K, CLOAD=50p
Wake up time	-	-	1	us	
Quiescent current	-	0.7	1.4	mA	
Maximum output voltage swing from rail		20		mV	V_{DD} =5.5, RL=10K
		100		mV	V_{DD} =5.5, RL=2K

6.4.9 Temperature Sensor

(V_{DD} - V_{SS} = 2.2 ~ 5.5 V ,T_A = -40~105°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
TA	Temperature	-40	-	105	℃	
-	Gain [1],	-	-1.81	-	mV/℃	
-	Offset [1,2]	-	715	-	mV	TA = 0 ℃

Note:

1. The temperature sensor formula for the output voltage (Vtemp) is list as below equation.
   Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)
2. The Gain and Offset may have some drift for different chips. Register SYS_TSOFFSET is a reference data measured by ADC in factory test.

6.4.10 ESD Characteristics

Symbol	Ratings	Condition	Package	Maximum Value	Unit
V_{ESD}	Electrostatic discharge (Human body mode)	TA = + 25 ℃	LQFP 48	6000	V
	Electrostatic discharge (Charged Device mode)			500	V

6.4.11 EFT Characteristics

Symbol	Condition	Package	Pass Level	Unit
	Fsys			
	HIRC	LQFP 48	+/- 4000	V

6.5 Flash DC Electrical Characteristics

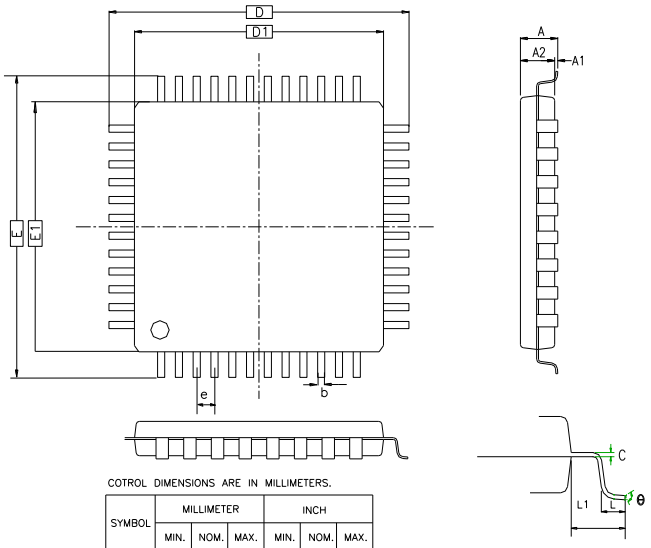
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.35	1.5	1.65	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A =85℃
T_{ERASE}	Sector Erase Time	-		5	ms	
T_{PROG}	Program Time	-	5	6.5	us	Per Byte
I_{DD1}	Read Current	-	4	5.5	mA	@50MHz
I_{DD2}	Program Current	-	-	3.5	mA	
I_{DD3}	Erase Current	-	-	2	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
   Guaranteed by design, not test in production.

7 PACKAGE DIMENSIONS

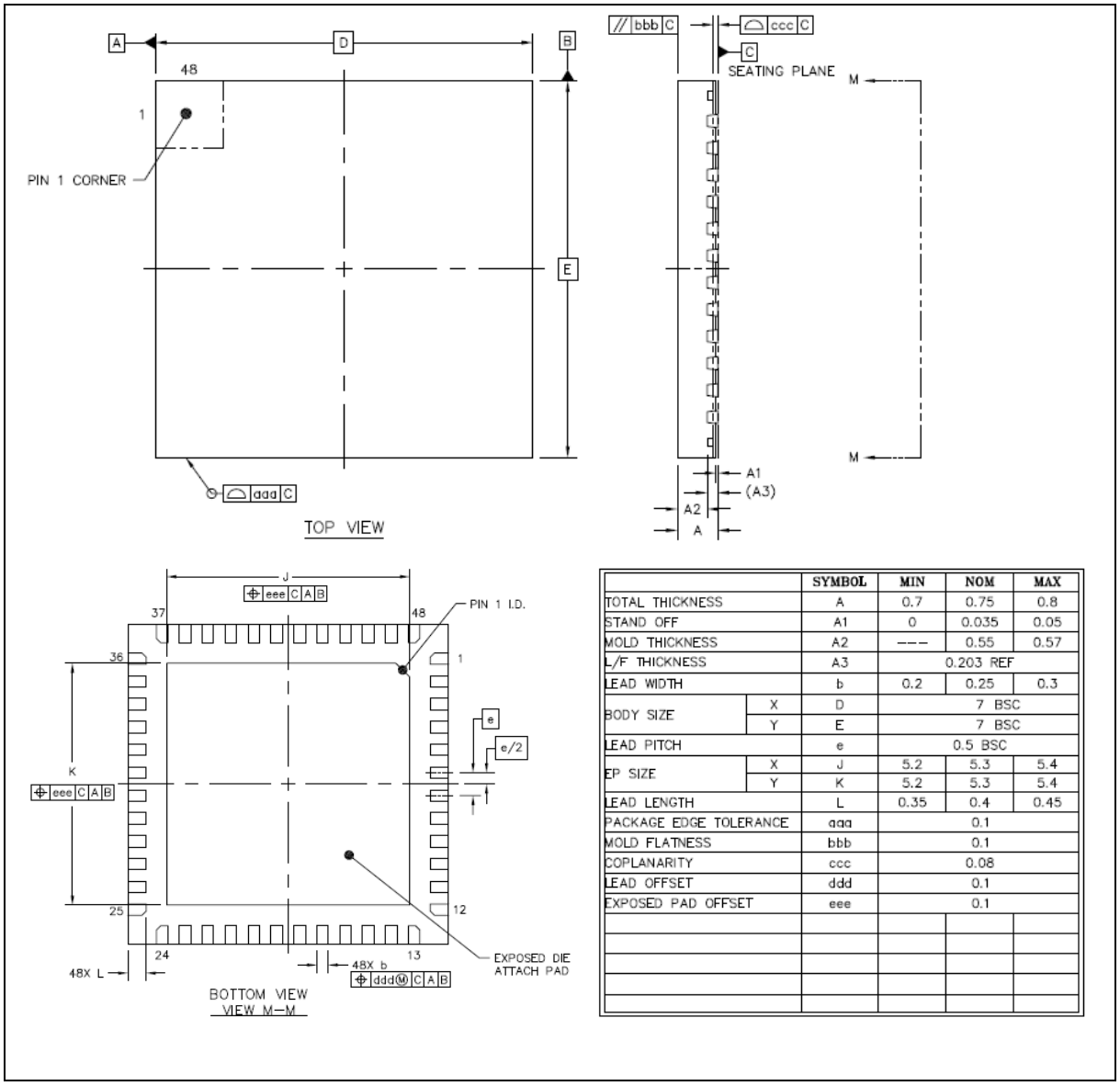
7.1 48-Pin LQFP 7x7mm



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

7.2 48-Pin QFN 7x7mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

8 REVISION HISTORY

Date	Revision	Description
2020.06.16	0.1	Preliminary version.
2020.12.08	0.1	Remove some parts including NM1233D, NM1233Y, NM1232D and NM1232Y.
2021.10.01	0.1	1. Update the ESD and EFT characteristics

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.