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1. GENERAL DESCRIPTION

The NUC501 is an ARM7TDMI-based MCU, specifically designed to offer low-cost and high-performance for various applications, like interactive toys, edutainment robots, and home appliances. It integrates the 32-bit RISC CPU with 32KB high-speed SRAM, crypo engine with OTP key, boot ROM, LDO regulator, ADC, DAC, I2C, SPI, USB2.0 FS Device, & GPIO into a cost-affordable whil feature-rich micro-controller.

Owing to the simplicity of the NUC501 architecture that boots SpiMemory[1] into the high-speed SRAM for program execution, the total system BOM is reduced to its minimum. Unlike usual ARM-based MCU products, the NUC501 operates without the use of SDRAM, which is usually the source of complexity, higher power consumption, and cost.

The ARM7TDMI runs up to 81MHz on the high-speed SRAM to offer enough horsepower for many MIPS-hungry tasks, while the remaining MIPS is still able to serve the need of application program. For those applications, like cartridge games, that require large code storage and variation of game play scenarios, the patented Extensible XIP Addressing on SpiMemory gives the flexibility whenever program execution speed is not a critical concern.

To protect the code against illegal pirating, the NUC501 provides a crypto engine that works with internal OTP[2] key to encrypt the data stored at external SpiMemory when the design-in is finished. Without the knowledge of the OTP key, others can't decrypt the data even by means of ICE debugging.

The NUC501 is designed with special care to minimize the power consumption while allowing for the flexibility to reach for high performance. It includes the clock gating, variable frequency control for individual IP's, and bus control to reduce signal toggle. Besides, the NUC501 can be further operated under different power-saving modes: idle, power down with RTC active, and power down mode.

With so many practical peripherals integrated around the high-performance ARM7 CPU, the NUC501 is suitable for such applications as Interactive toys, edutainment robots, and home appliances. Whenever MIPS-hungry task meets cost-effective demand, you'll find the NUC501 truly useful to satisfy the requirement.

1.1 Applications

Edutainment Robots

Home Appliances

Proprietary RF BB

[1] SpiMemory denotes the industry standard SPI interfaced memory devices, like SpiFlash, SpiROM, etc.

[2] OTP means One Time Programmable EPROM, which can only be programmed once.

2. FEATURES

- 32-bit RISC CPU based on ARM7TDMI @ 81 MHz
- 16-bit Thumb mode supported to save code size
- Embedded 32 KB Local Memory divided into 16 segments for easier S/W programming
- Boot from SpiMemory or USB
- Program download into SRAM through JTAG before OTP key programmed
- Integrate JTAG port to support real time, non-stop ICE function for system development and debugging
- 6KB internal ROM for Boot loader
- ICP[3] for programming SpiFlash & OTP key via USB
- 32KB internal SRAM
- Embedded 32KB high-speed SRAM for code + data.
- SpiMemory interface with code protection
- DMA mode for code booting from SpiMemory to SRAM
- Direct CPU read access mode from SpiMemory.
- 128-bit OTP key for code protection against illegal pirating
- 2-bit SPI mode supported for doubling data transfer rate
- Shared (when not in use) with other SPI device for high-speed transfer via DMA
- Audio Process Unit
- Mono 16-bit Sigma-Delta DAC output
- Equalization function supported
- USB 2.0 Full-Speed device
- 6 programmable endpoints for Control, Bulk In/Out, Interrupt and Isochronous transfers
- 512-byte USB buffer
- Auto suspend function
- Remote wakeup capability
- I^2C Compatible with Philips I^2C standard
- Programmable SPI master/slave mode Speed up to 40MHz

[3] ICP: In Circuit Programming, which means the capability to upgrade code with IBR on target board directly.

- 4 Channel PWM with Four 16-bit timers, programmable duty control of output waveform (PWM), auto reload mode or one-shot pulse mode, capture and compare function.
- Analog to Digital Converter includes 10-bit x 8-ch ADC for sensor, MIC, LVD, LVR.
- Maximum ADC conversion rate: 400K samples per second.
- ADC Power supply voltage: 3.3V and analog input voltage range: 0 ~ 3.3 volts
- ADC support wait-for-trigger mode & standby mode
- Dedicated LVD / LVR with 8-level voltage detection
- Two programmable 32-bit timers with 8-bit pre-scaler, one 32-bit watch dog timer
- 32.768KHz RTC function support
- Up to 26 / 37 GPIO pins for LQFP-48 / LQFP-64
- Two UART ports with flow control (TX, RX, CTS and RTS)
- Power management modes: normal, idle, power down with RTC, & power down.
- 3.3V to 1.8V 200mA LDO regulator
- Technology & Package
- 0.18um CMOS
- 3.3-volt single supply
- LQFP-48 (NUC501ADN) / LQFP-64 (NUC501BDN)

3. PIN CONFIGURATION

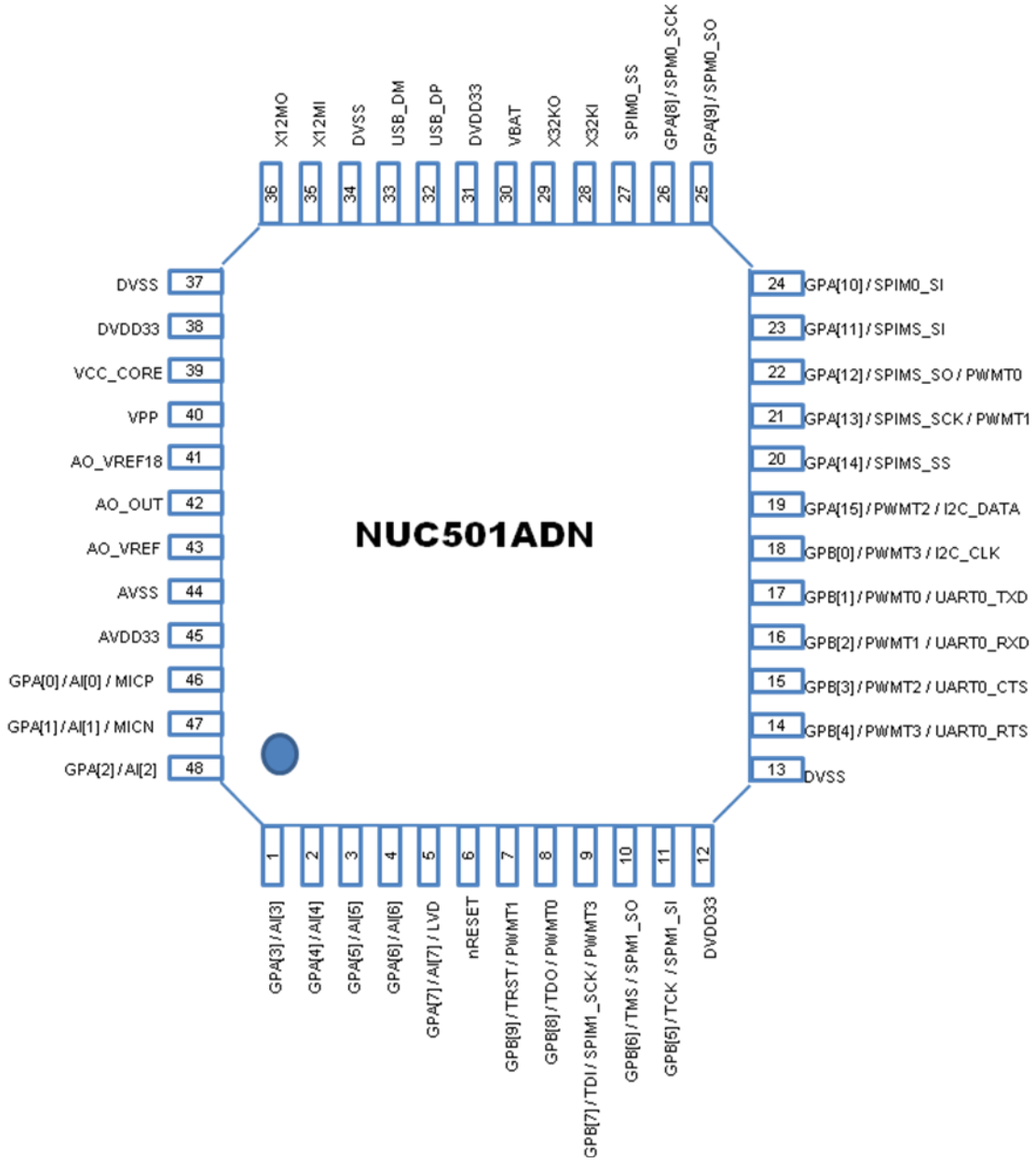


Fig. 1 LQFP-48 Pin Out

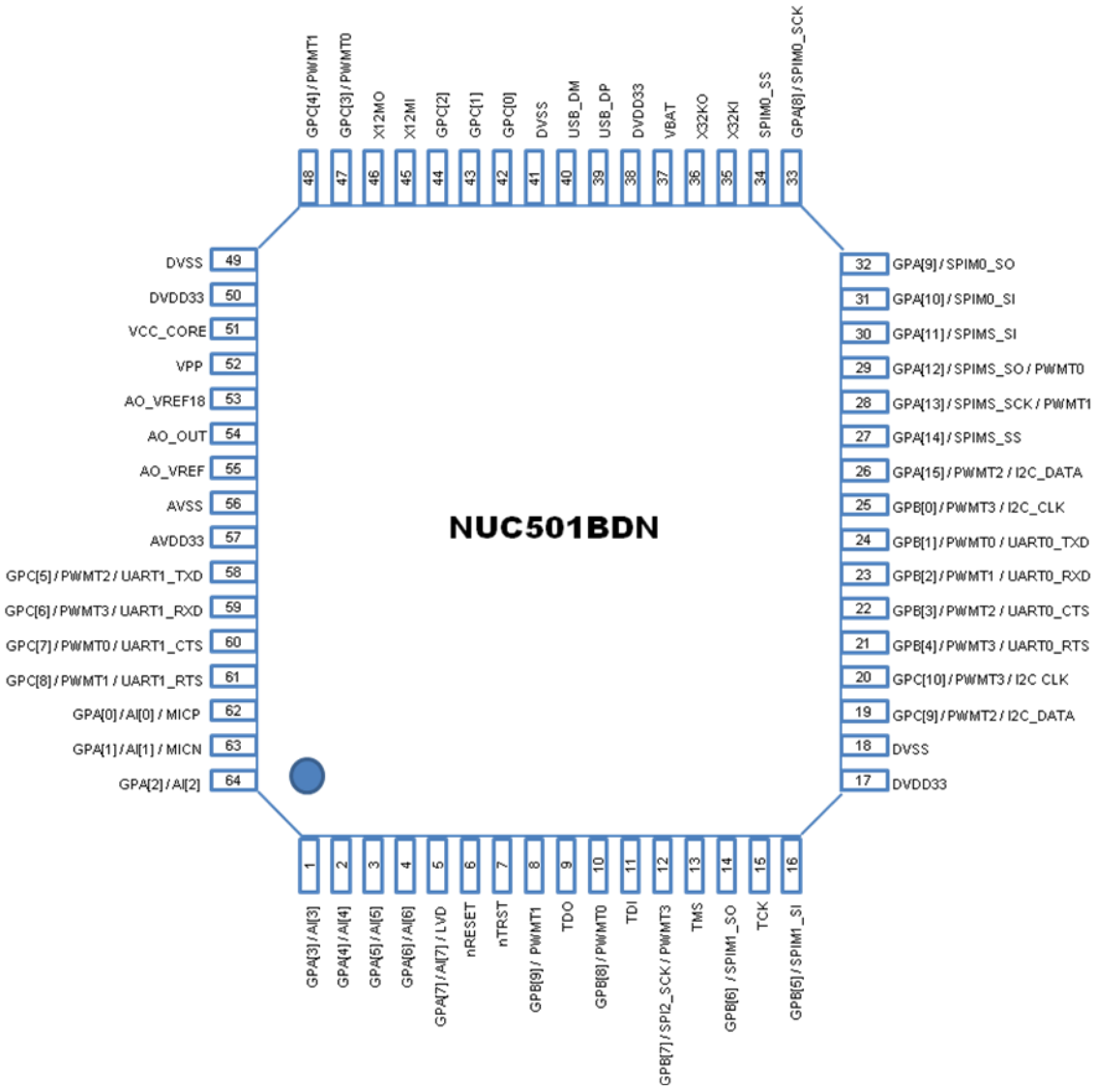


Fig. 2 LQFP-64 Pin Out

4. PIN DESCRIPTION

Symbol	LQFP-64	LQFP-48	TYPE	Description
GPA[0] / AI[0] / MICP	62	46	4/8 mA I/O I I	GPA[0] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[0] – ADC analog input 0 MICP – Microphone input +
GPA[1] / AI[1] / MICN	63	47	4/8 mA I/O I I	GPA[1] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[1] – ADC analog input 1 MICN – Microphone input -
GPA[2] / AI[2]	64	48	4/8 mA I/O I	GPA[2] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[2] – ADC analog input 2
GPA[3] / AI[3]	1	1	4/8 mA I/O I	GPA[3] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[3] – ADC analog input 3
GPA[4]/ AI[4]	2	2	4/8 mA I/O I	GPA[4] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[4] – ADC analog input 4
GPA[5] / AI[5]	3	3	I/O I	GPA[5] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[5] – ADC analog input 5
GPA[6] / AI[6]	4	4	4/8 mA I/O I	GPA[6] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[6] – ADC analog input 6
GPA[7] / AI[7] / LVD	5	5	4/8 mA I/O I I	GPA[7] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. AI[7] – ADC analog input 7 LVD – Low Voltage Detection
GPA[8] / SPIM0_SCK	33	26	4/8 mA I/O O	GPA[8] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIM0_SCK – Serial clock output pin for SPI0

GPA[9] / SPIM0_SO	32	25	4/8 mA I/O I/O	GPA[9] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIM0_SO – Serial data input/output pin for SPIM0. In normal SPI mode, this pin is used as data out. In fast SPI read mode, this pin is the 2nd bit for data in. The fast read mode can accelerate the SPI read data rate.
GPA[10] / SPIM0_SI	31	24	4/8 mA I/O I	GPA[10] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIM0_SI – Serial data input pin for SPIM0.
GPA[11] / SPIMS_SI	30	23	4/8 mA I/O I	GPA[11] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIMS_SI – Serial data input pin for SPIMS.
GPA[12] / SPIMS_SO / PWMT0	29	22	4/8 mA I/O O O	GPA[12] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIMS_SO – Serial data output pin for SPIMS. PWMT0 – PWM output for timer 0
GPA[13] / SPIMS_SCK / PWMT1	28	21	4/8 mA I/O O O	GPA[13] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIMS_SCK – Serial clock pin for SPIMS. PWMT1 – PWM output for timer 1
GPA[14] / SPIMS_SS / USB_DET	27	20	4/8 mA I/O O I	GPA[14] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIMS_SS - Serial chip select pin for SPIMS. USB_DET – USB detected pin
GPA[15] / PWMT2 / USB_DET / IC2_DATA	26	19	4/8 mA I/O O I I/O	GPA[15] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT2 – PWM output for timer 2. USB_DET – USB detected pin. I2C_DATA – I2C data input/output pin.
GPB[0] / PWMT3 / USB_DET / I2C_CLK	25	18	4/8 mA I/O O I O	GPB[0] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT3 – PWM output for timer 3 . USB_DET – USB detected input I2C_CLK – I2C data output pin
GPB[1] /	24	17	12/16	GPB[1] – General purpose input/output digital pin with drive/sink

			mA I/O	capability @ 12 / 16 mA.
PWMT0 /			O	PWMT0. – PWM output for timer 0
USB_DET /			I	USB_DET – USB detected input
UART0_TXD			O	UART0_TXD – Data transmitter output pin for UART0
GPB[2] /	23	16	12/16 mA I/O	GPB[2] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.
PWMT1 /			O	PWMT1 – PWM output for timer 1.
USB_DET /			I	USB_DET – USB detected input
UART0_RXD			I	UART0_RXD – Data receiver input pin for UART0
GPB[3] /	22	15	12/16 mA I/O	GPB[3] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.
PWMT2 /			O	PWMT2 – PWM output for timer 2
USB_DET /			I	USB_DET – USB detected input
UART0_CTS			I	UART0_CTS – Clear to Send input pin for UART0
GPB[4] /	21	14	12/16 mA I/O	GPB[4] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.
PWMT3 /			O	PWMT3 – PWM output for timer 3
USB_DET /			I	USB_DET – USB detected input
UART0_RTS			O	UART0_RTS – Request to Send output pin for UART0
GPB[5] /	16	11	12/16 mA I/O	GPB[5] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.
TCK /			I	TCK – JTAG ICE Test Clock pin (LQFP-48 only)
SPIM1_SI			I	SPIM1_SI – Serial data input pin for SPIM1
GPB[6] /	14	10	12/16 mA I/O	GPB[6] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.
TMS /			I	TMS – JTAG ICE Test Mode Select pin (LQFP-48 only)
SPIM1_SO/			O	SPIM1_SO – Serial data output pin for SPIM1
PWMT2			O	PWMT2 – PWM output for timer 2.
GPB[7] /	12	9	12/16 mA I/O	GPB[7] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.
TDI /			I	TDI – JTAG ICE TDI pin (LQFP-48 only)
SPIM1_SCK /			O	SPIM1_SCK – Serial clock output pin for SPIM1
PWTM3			O	PWMT3 – PWM output for timer 3
GPB[8] /	10	8	12/16 mA I/O	GPB[8] – General purpose input/output digital pin with drive/sink capability @ 12 / 16 mA.

TDO / USB_DET / PWMT0			I O	TDO – JTAG ICE TDO interface (LQFP-48 only) USB_DET – USB detected input PWMT0 – PWM output for timer 0
GPB[9] / nTRST / USB_DET / PWMT1	8	7	4/8 mA I/O I I O	GPB[9] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. nTRST – JTAG ICE reset pin (LQFP-48 only) USB_DET – USB detected input PWMT1 – PWM output for timer 1.
GPC[0] / SPIM1_S0 / USB_DET	42	NC	4/8 mA I/O O I	GPC[0] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIM1_SO – Serial data output pin for SPIM1 USB_DET – USB detected input
GPC[1] / SPIM1_SI / USB_DET	43	NC	4/8 mA I/O I I	GPC[1] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIM1_SI – Serial data input pin for SPIM1 USB_DET– USB detected input
GPC[2] / SPIM1_SCK / USB_DET	44	NC	4/8 mA I/O O I	GPC[2] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. SPIM1_SCK – Serial clock output pin for SPIM1 USB_DET – USB detected input
GPC[3] / PWMT0 / USB_DET	47	NC	4/8 mA I/O O I	GPC[3] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT0 – PWM output for timer 0 USB_DET– USB detected input
GPC[4] / PWMT1 / USB_DET	48	NC	4/8 mA I/O O I	GPC[4] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT1 – PWM output for timer 1 USB_DET – USB detected input
GPC[5] / PWMT2 / UART1_TXD	58	NC	4/8 mA I/O O O	GPC[5] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT2 – PWM output for timer 2 UART1_TXD – Data transmitter output pin for UART1

GPC[6] / PWMT3 / UART1_RXD	59	NC	4/8 mA I/O O I	GPC[6] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT3 – PWM output for timer 3 UART1_RXD – Data Receiver input pin for UART1
GPC[7] / PWMT0 / UART1_CTS	60	NC	4/8 mA I/O O I	GPC[7] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT0– PWM output for timer 0 UART0_CTS – Clear to Send input pin for UART1
GPC[8] / PWMT1 / USRT1_RTS	61	NC	4/8 mA I/O O O	GPC[8] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT1 – PWM output for timer 1 UART1_RTS – Request to Send output pin for UART1
GPC[9] / PWMT2 / I2C_DATA	19	NC	4/8 mA I/O O I/O	GPC[9] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT2 – PWM output for timer 2 I2C_DATA – I2C data input/output pin
GPC[10] / PWMT3 / I2C_CLK	20	NC	4/8 mA I/O O O	GPC[10] – General purpose input/output digital pin with drive/sink capability @ 4 / 8 mA. PWMT3 – PWM output for timer 3 I2C_CLK – I2C data output pin
SPIM0_SS	34	27	O	Chip Select pin for SPIM0 to connect with SpiMemory
USB_DP	39	32	I/O	USB2.0 Full Speed signal D+
USB_DM	40	33	I/O	USB2.0 Full Speed signal D-
X12MI	45	35	I	Crystal input pin
X12MO	46	36	O	Crystal output pin
X32KI	35	28	I	RTC 32.768KHz crystal input pin
X32KO	36	29	O	RTC 32.768KHz crystal output pin
nRESET	6	6	I	External reset input – Low active, set this pin low will reset NUC501 to initial state
TCK	15	NC	I	JTAG ICE Test Clock pin
TMS	13	NC	I	JTAG ICE Test Mode Select pin
nTRST	7	NC	I	JTAG ICE Reset pin

TDO	9	NC	O	JTAG ICE TDO interface
TDI	11	NC	I	JTAG ICE TDI interface
AO_OUT	54	42	A	Voltage-type audio DAC output pin. Connect to external PA (Power Amplifier).
AO_VREF18	53	41	P	1.8V power for analog circuit . Connect to VCC_CORE.
AO_VREF	55	43	A	Analog circuit voltage reference pin. Requires external capacitors of at least 0.1uF between AO_VREF and DVSS.
DVDD33	17, 38, 50	12, 31, 38	P	3.3V power supply for I/O ports and LDO source for internal PLL and digital circuit
AVDD33	57	45	P	3.3V power supply for for internal analog circuit
VCC_CORE	51	39	P	LDO 1.8V output pin. Requires one external capacitor of at least 47μF between VCC_CORE and DVSS.
VBAT	37	30	P	RTC Power supply: 1.2V ~ 1.8V
VPP	52	40	P	OTP VPP pin. For programming OTP, this pin requires typical 6.5V. For read, this pin should be kept at 1.8V.
DVSS	18, 41, 49	13, 34, 37	G	Ground Pin for digital circuit
AVSS	56	44	G	Ground Pin for analog circuit

Note: I – Input, O – Output, I/O – Input/Output, P – Power, G – Ground, A – Analog.

5. SYSTEM DIAGRAM

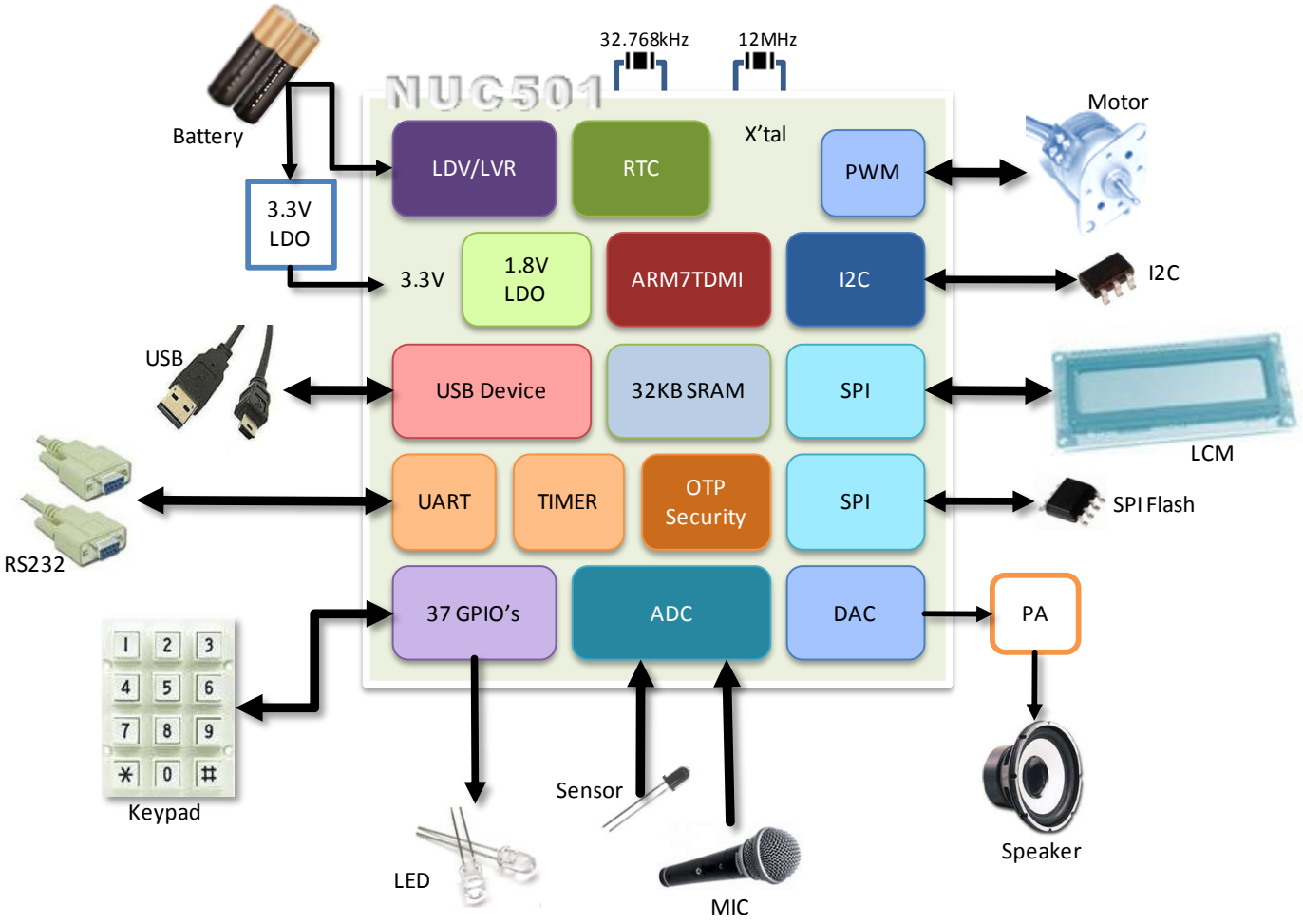


Fig. 3 System Block Diagram

6. BLOCK DIAGRAM

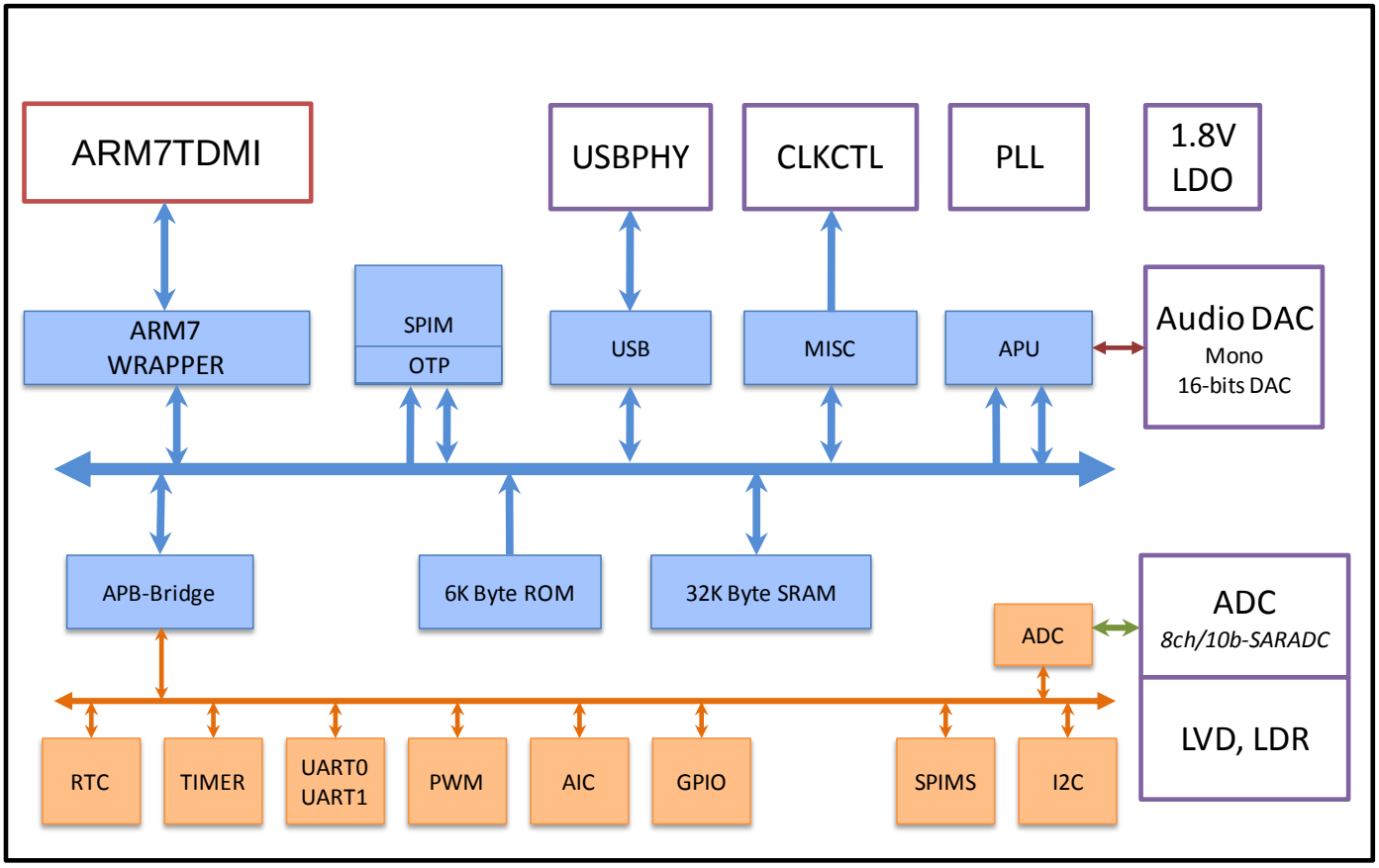


Fig. 4 Block Diagram

7. FUNCTIONAL DESCRIPTION

7.1 ARM7TDMI CPU Core

The ARM7TDMI CPU core, a member of the Advanced RISC Machines (ARM) family of general-purpose 32-bit microprocessors, offers high performance with very low power consumption. The architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro-programmed Complex Instruction Set Computers. Pipelining is employed so that all parts of the processing and memory systems can operate continuously. The high instruction throughput and impressive real-time interrupt response are the major benefits.

The ARM7TDMI CPU core has two instruction sets:

(1) Standard 32-bit ARM set
(2) 16-bit THUMB set

The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM core while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. THUMB instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and THUMB states. Each 16-bit THUMB instruction has a corresponding 32-bit ARM instruction with the same effect on the processor model.

ARM7TDMI CPU core has 31 x 32-bit registers. At any one time, 16 sets are visible; the other registers are used to speed up exception processing. All the register specifies in ARM instructions can address any of the 16 registers. The CPU also supports 5 types of exception, such as two levels of interrupt, memory aborts, attempted execution of an undefined instruction and software interrupts.

7.2 Power-On Settings

The power-on setting is used to configure the chip to enter the specified state when the chip is powered up or reset. Since each pin of power on setting has an internal pulled-up resistor. If the application needs to set the configuration to "0", the proper pull-down resistor of 10 KOhm must be added for the corresponding configuration pins.

Pin Name	Descriptions	**Register Bit Mapping**
GPB[8] GPB[4]	SPI flash speed selection	SPOCR [6:5]
GPB[1]	ICE Mode configuration setting "0" – ICE mode and Crypto function disabled "1" – Normal mode	SPOCR [4]

GPA[13]	LQFP-48 ICE mode configuration setting "1" – GPB[9:5] as normal function "0" – GPB[9:5] as ICE pins	SPOCR [3]
GPA[12] GPA[9] GPA[8]	3'b000 : test mode 3'b001 : test mode 3'b010 : test mode 3'b011 : test mode 3'b100 : Boot from SRAM 3'b101 : Boot from USB 3'b110 : OTP program mode 3'b111 : Boot from SpiMemory	SPOCR[2:0]

7.3 SRAM

The embedded high-speed SRAM is designed for both program code and scrachpad data RAM. It's 32KB on the AHB bus and is divided into 16 memory blocks with 2KB each. Each memory block can be randomly mapped to any 2KB space of 0x0000_0000 ~ 0x1FFF_FFFF of system memory by modifying the control register. Each 2KB memory block can also be disabled individually by modifying the control register.

At default, these 16 x 2KB memory blocks are all enabled and mapped to 0x0000_0000 ~ 0x0000_7FFF sequentially.

7.4 Memory Mapping

The NUC501 always boot from IBR (Internal Boot ROM), which is used to move the code to internal high-speed SRAM either from SpiMemory or USB. Thereafter, the NUC501 will re-boot from address 0x0000-0000 of the re-mapped memory space, as shown in Fig. 5 Memory Mapping.

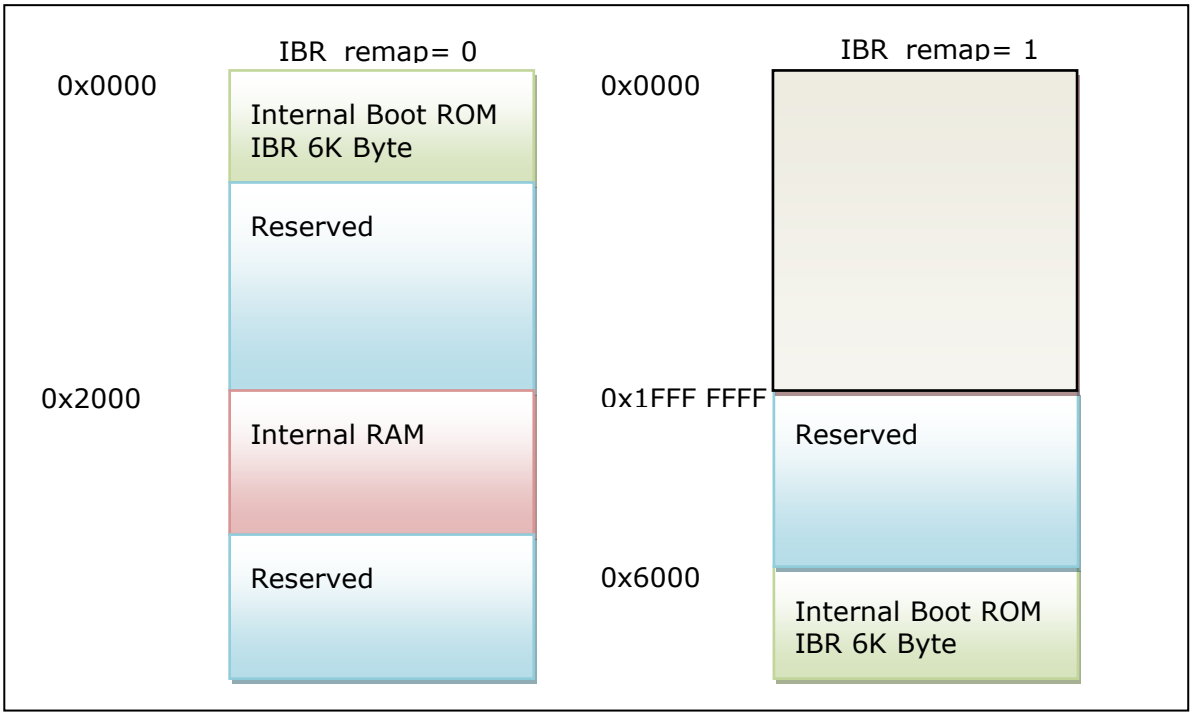


Fig. 5 Memory Mapping

7.5 Analog To Digital Converter

The 10-bit ADC (Analog to Digital Converter) is a successive approximation type ADC with 8-channel inputs. Two input pins (AI[0] & AI[1]) are dedicated to connecting with differential MIC for voice recording.

It needs 50 cycles to convert one sample. With the maximum input clock to ADC @ 25MHz, the maximum conversion rate is 400K/sec. The operating voltage range is 3.3V +/- 10% with power down mode supported.

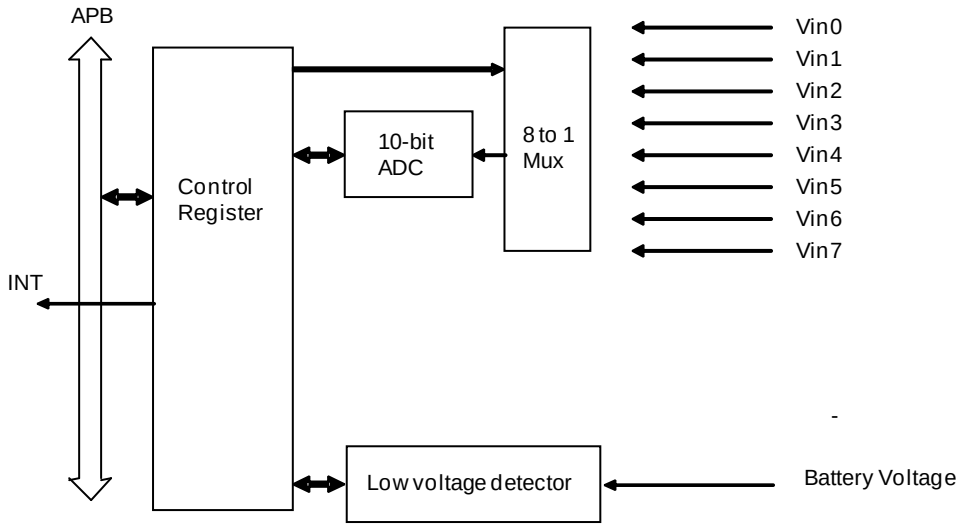


Fig. 6 ADC Block Diagram

Beside the 10-bit ADC, an 8-level voltage detector is also included. The result of this LVD is independent of power supply, which would send out the warning signal when battery voltage is lower than an absolute reference voltage.

7.5.1 Voltage detector

The architecture of the voltage detector is shown as in the following figure.

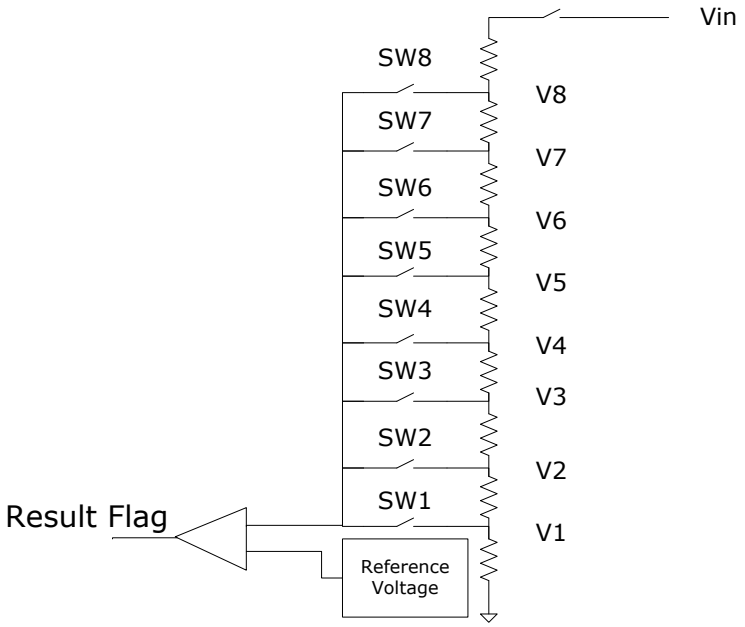


Fig. 7 Architecture of Voltage Detector

7.5.2 Recording path

The MIC recording path converts the analog audio signal into ditial form by means of the ADC. When the recording path is in use, other channels for data conversion @ ADC can't operate lest noise coupling would deteriorate the S/N ratio.

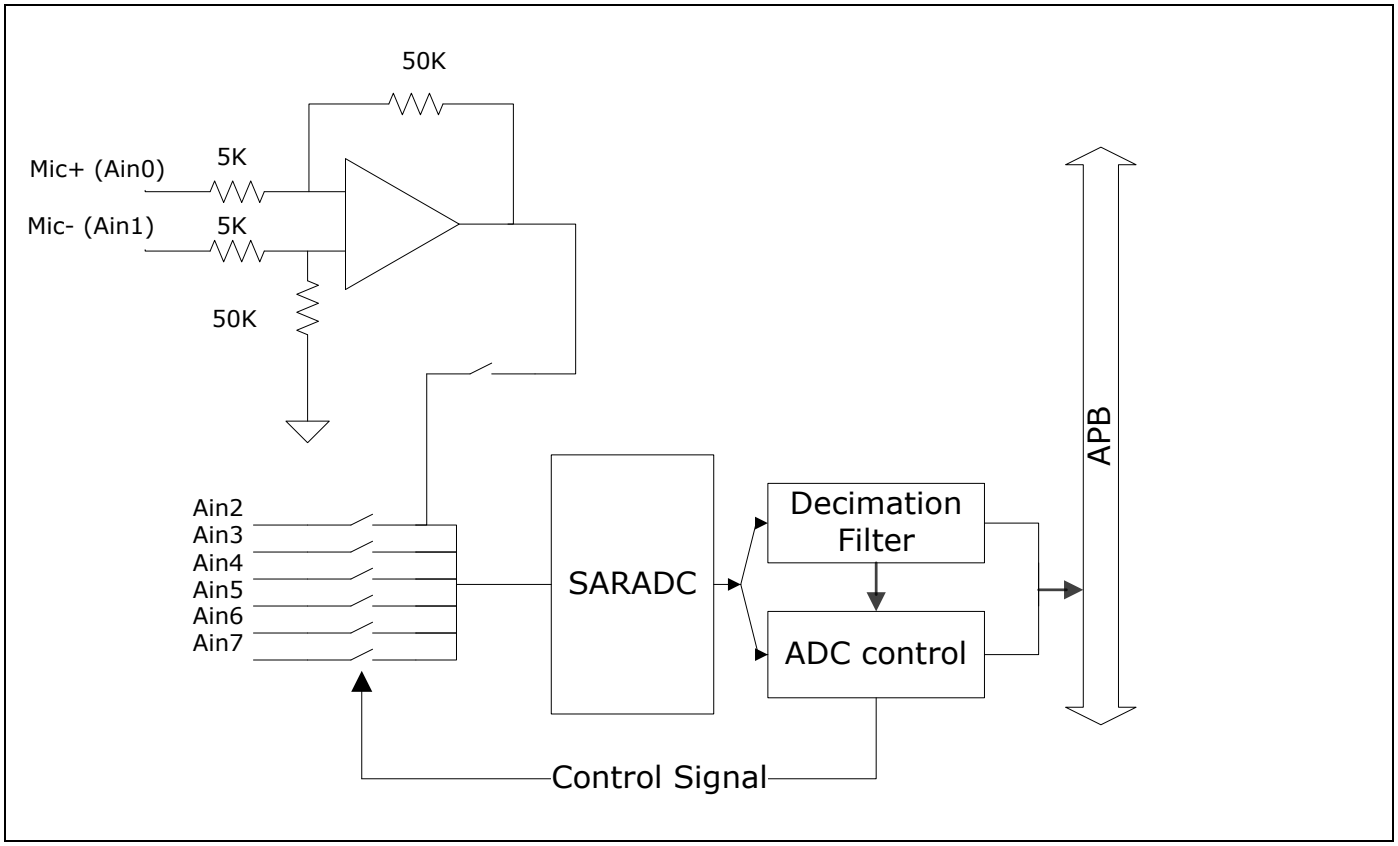


Fig. 8 SAR ADC Block Diagram

7.6 Audio Processing Unit (APU)

The APU is a master device on the AHB bus with built-in 16-Byte FIFO & timer. It's used to playback the audio data (in PCM format), which is previously decoded and stored in global RAM by the ARM7 CPU. The APU is built–in with a monophonic DAC @ 16-bit resolution.

7.7 Write-Back & Content Download @ SpiFlash

SpiFlash provide sector erase (4KB) and page program (256 byte) command.NUC501 provide SPI software library for data write back to SpiFlash. NUC501 can use USB and ARM CPU to write back data to SpiFlash.

7.8 OTP Key Programming

The OTP content is unknown upon power on. When the system is powered up and booted from IBR (Internal Boot ROM), the OTP is read out once to check the OTP status. It's necessary to program the OTP key before the crypto engine can be enabled.

If the OTP is non-programmed, IBR can follow the programming step to program the OTP. During OTP programming, IBR will use a GPIO pin to control external power switch for applying either 1.8v or 6.5v to the VPP pin.

Nuvoton provides the following ways in OTP programming:

OTP key programming @ CP test for large-quantity demand before shipping

Schematics for test fixture @ mass production of COB.

Gang writer for LQFP packages.

7.9 Clock Controller

The clock controller generates the clocks for the whole chip, it include all AMBA interface modules and all peripheral clocks, the USB, UART, APU and so on. There is one PLL module in this chip, and the PLL clock source is input from the external crystal.

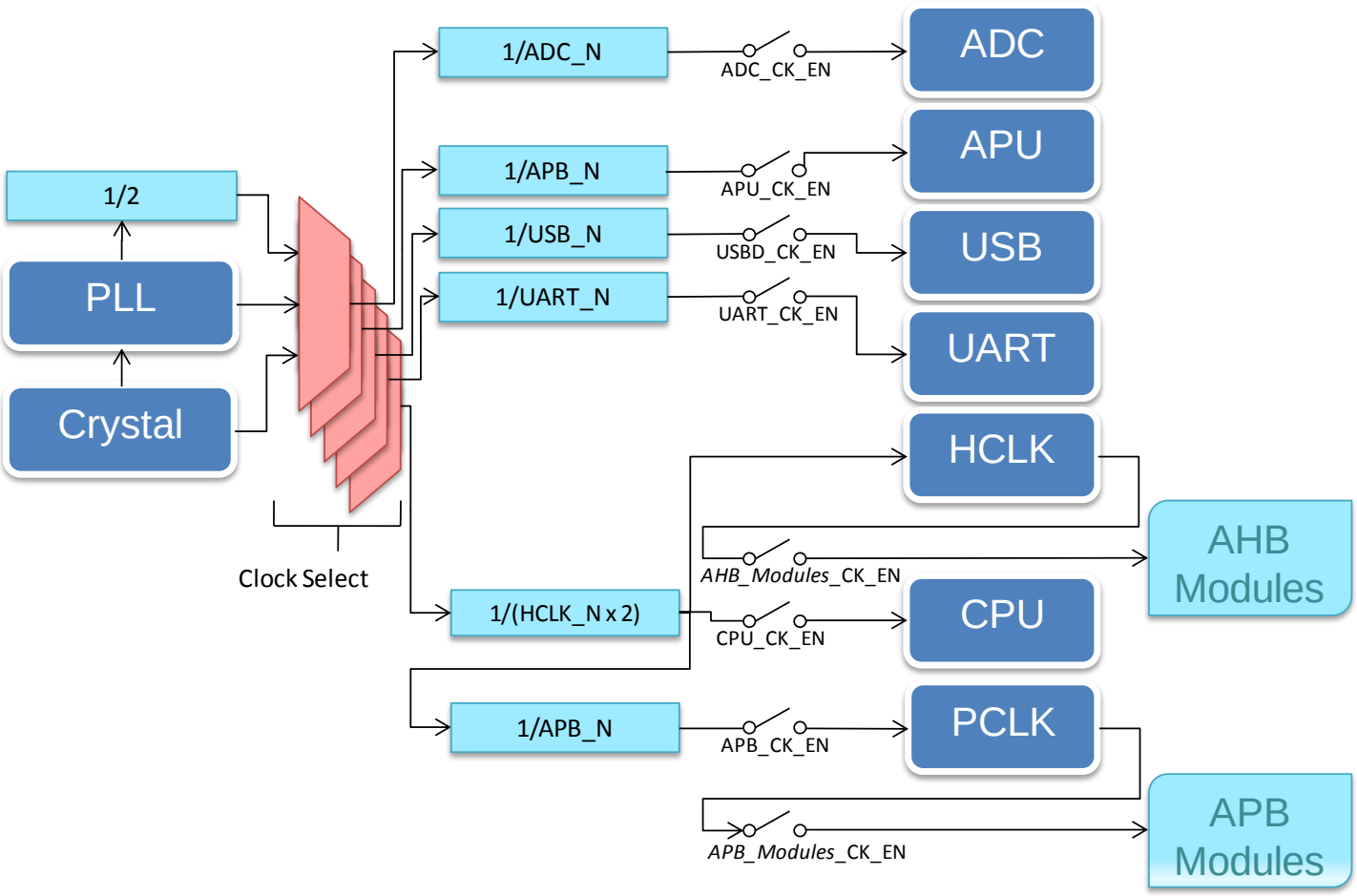


Fig. 9 Clock Controller Block Diagram

The clock controller implements the power control function, include the individually clock on or off control register, clock source select and the divior number to get the required clock. These functions minimize the power consumption and the chip runs on the proper condition. In power down mode, the controller turns off the crystal oscillator to minimize the power consumption.

The clock HCLK is the source for all the AMBA's modules. The HCLK is the operating clock for the SRAM and it is obtained by dividing by two from one of the sources: Crystal, PLL, PLL/2 or

32KHz crystal. The HCLK is used for the AMBA AHB BUS clock, ARM7 CPU, and the APB clock source.

7.10 Power control

The NUC501 supports two power-saving modes: Idle and Powe-down mode.

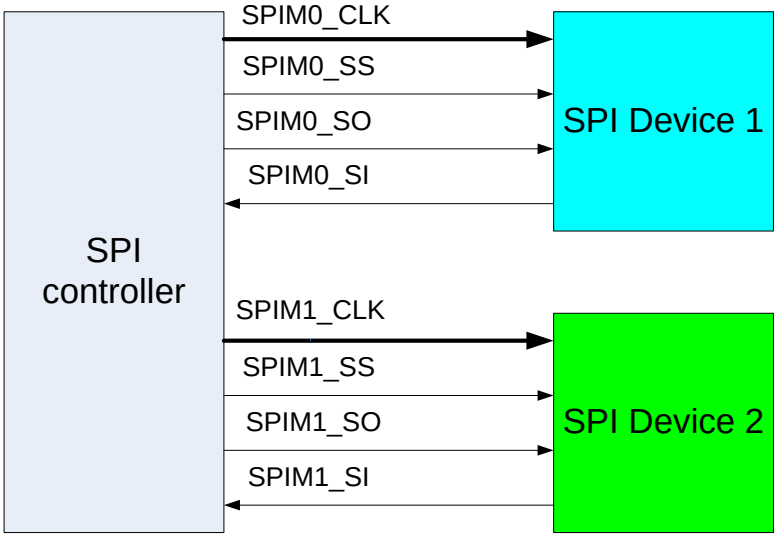
Idle mode – The CPU clock is stopped, some peripheral functions would continue operation during Idle mode and can wake-up the CPU when external interrupts occur.

Power-down mode – All clocks and peripherals are stopped. The oscillator is shut down and the chip receives no internal clocks. The Power-down mode can be terminated and normal operation to resume upon certain specific interrupts that requires no clock. Power-down mode is intended to archieve the lowest possible power consumption. RTC can be kept alive for keeping the time base, either powered from the internal LDO or a single-cell separate battery.

7.11 SPI Master Controller

The SPI (Serial Peripheral Interface) master controller performs a serial-to-parallel conversion on data characters received from the peripheral, and a parallel-to-serial conversion on data characters received from CPU. This controller can drive up to 2 external peripherals, but is time-shared and can not operate simultaneously. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The slave select signal can be chosen to be low active or high active. Writing a divisor into the DIVIDER register can program the frequency of serial clock output. This master core contains four 32-bit transmit/receive buffers, and can provide burst mode operation. It supports variable length transfer and the maximum transmit/receive length can be up to 128 bits. The full duplex, synchronous serial data transfer with MSB or LSB first option is supported.

Due to the limited 32KB SRAM space (for code + data), the extensible XIP space @ SpiMemory is useful for those applications that do not require high-speed program execution. Customers can put program code in the SpiMemory along with other data types and XIP (Execute In Place) from the external memory directly.



7.12 SPI Master/Slave Controller

The SPI master/slave controller is similar to the SPI master mentioned above. It contains four 32-bit transmit/receive buffers to provide burst mode operation. It supports variable length transfer and the maximum transmit/receive length can be up to 128 bits.

It can be selected as master or slave device.

7.13 PWM (Pulse Width Modulation)

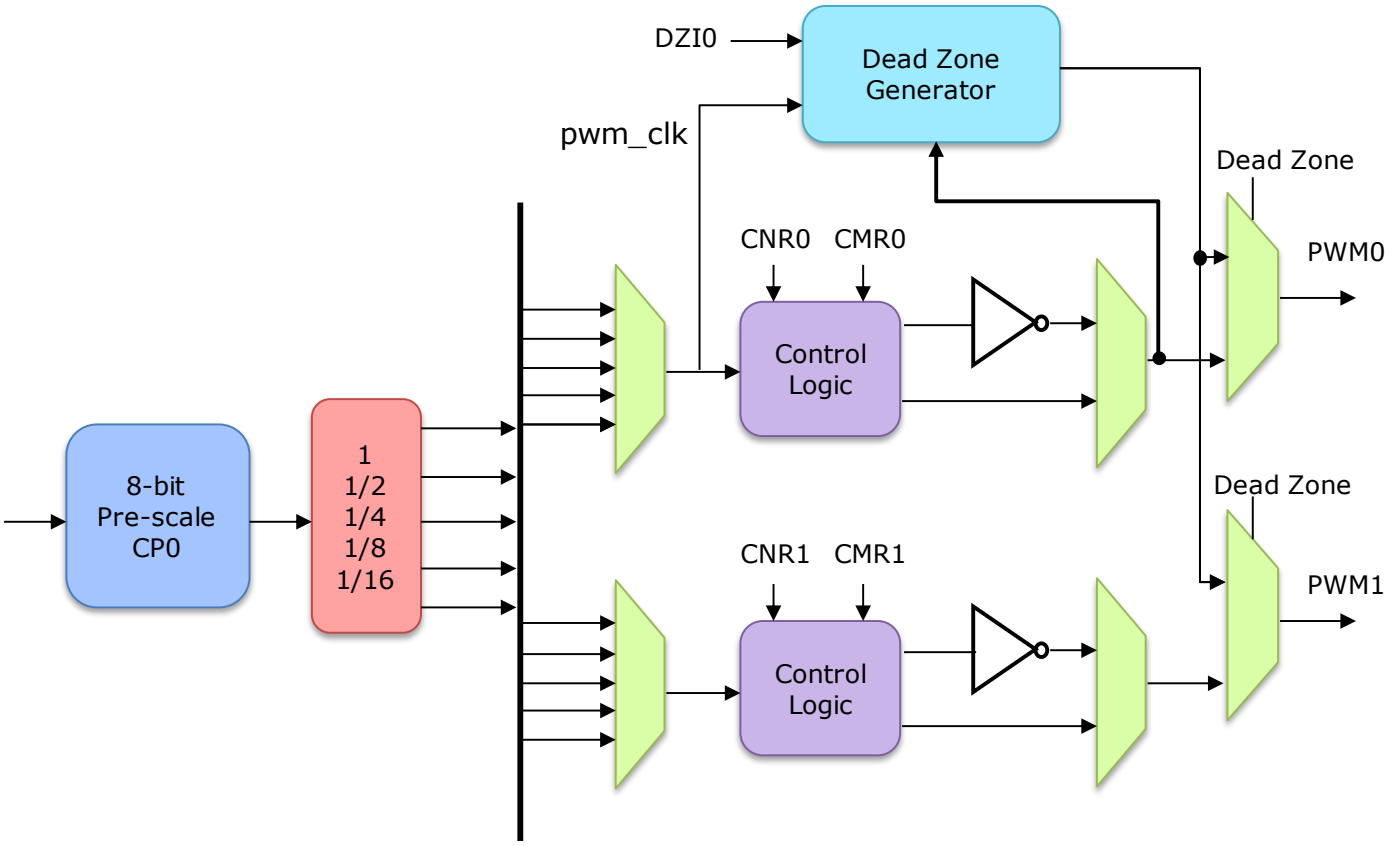


Fig. 10 PWM Block Diagram

The NUC501 have 4 PWM timers, which got 2 Prescaler, 2 clock dividers, 4 clock selectors, 4 16-bit counters, and 4 16-bit comparators. They are all driven by the system clock. Each can be used as a timer and issue interrupt independently.

Each two PWM timers share one prescaler (0/1 share prescale0 and 2/3 share prescale1). Clock divider provides each timer with 5 clock sources (1, 1/2, 1/4, 1/8, 1/16). Each timer receives its own clock signal from clock divider, which receives clock from 8-bit prescaler. The 16-bit counter in each timer receives clock signal from clock selector and can be used to handle one PWM period. The 16-bit comparator compares number in counter with threshold number in register loaded previously to generate PWM duty cycle.

When 16-bit down counter reaches zero, the interrupt request is generated to inform CPU that time is up. When counter reaches zero, if counter is set as toggle mode, it is reloaded automatically and start to generate next cycle. User can set counter as one-shot mode instead

of toggle mode. If counter is set as one-shot mode, counter will stop and generate one interrupt request when it reaches zero.

The value of comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

There are only four interrupts from PWM to advanced interrupt controller (AIC). PWM 0 and Capture 0 share the same interrupt, PWM1 and Capture 1 share the same interrupt and so on. Therefore, PWM function and Capture function in the same channel cannot be used at the same time.

7.14 I2C (Inter-Integrated Circuit) Bus Controller

Serial, 8-bit oriented bi-directional data transfers can be made up to 100 kbit/s in Standard-mode, up to 400 kbit/s in the Fast-mode. Only 100kbps and 400kbps modes are supported directly.

The I^2C Master Core includes the following features:

- Compatible with Philips I^2C standard, support master mode
- Clock stretching and wait state generation
- Provide multi-byte transmit operation, up to 4 bytes can be transmitted in a single transfer
- Software programmable acknowledge bit
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Software mode I2C supported

7.15 RTC (Real Time Clock)

RTC can be operated by independent power supply @ VBAT = 1.2 ~ 1.8V, while the system power (say adaptor from AC outlet) is off. The RTC uses a 32.768 KHz external crystal. A built-in RTC is designed to generate periodic interrupt signals at the interval of 1/128 ~ 1 second. The RTC oscillator is always enabled once powered on.

The RTC is embedded with hardware calendar function that supports from second up to year. CPU wake-up function supported as well.

7.16 AIC (Advanced Interrupt Controller)

An interrupt temporarily changes the execution sequence of a program to react to a particular event such as power failure, watchdog timer timeout, engine complete, system events, external event trigger and so on. The ARM processor provides two modes of interrupts, the Fast Interrupt (FIQ) mode for critical session and the Interrupt (IRQ) mode for general sessions. The IRQ exception occurs when the nIRQ input is asserted. Similarly, the FIQ exception occurs when the nFIQ input is asserted. The FIQ has privilege over the IRQ and can preempt an ongoing IRQ. It is possible to ignore the FIQ and the IRQ by setting the F-bit and I-bit in the current program status register (CPSR).

- External interrupts can be programmed as either edge-triggered or level-sensitive
- External interrupts can be programmed as either low-active or high-active
- Flags to reflect the status of each interrupt source

- Proprietary 8-level interrupt scheme to ease the burden from the interrupt
- Diasy-chain priority mechanism is applied to interrupts set as the same priority level.
- Automatically masking out the lower priority interrupt during interrupt nesting
- Automatically clearing the interrupt flag when the external interrupt source is programmed to be edge-triggered

7.17 GPIO (General Purpose I/O)

The NUC501 provide up to 37 GPIO pins (for LQFP-64), which are shared by multiple functions. In **Fig. 11 GPIO Block Diagram**, it shows how the GPIO configuration can be controlled through various registers. Each GPIO pin can be programmed to be Input, Ouput, pull-up resistor enable/disable, and drive capability selection (4mA / 8mA , 12mA / 16mA). The GPB[1:8] is specially designed to drive/sink LED without external drivers, so that it can be programmed to 12mA / 16mA.

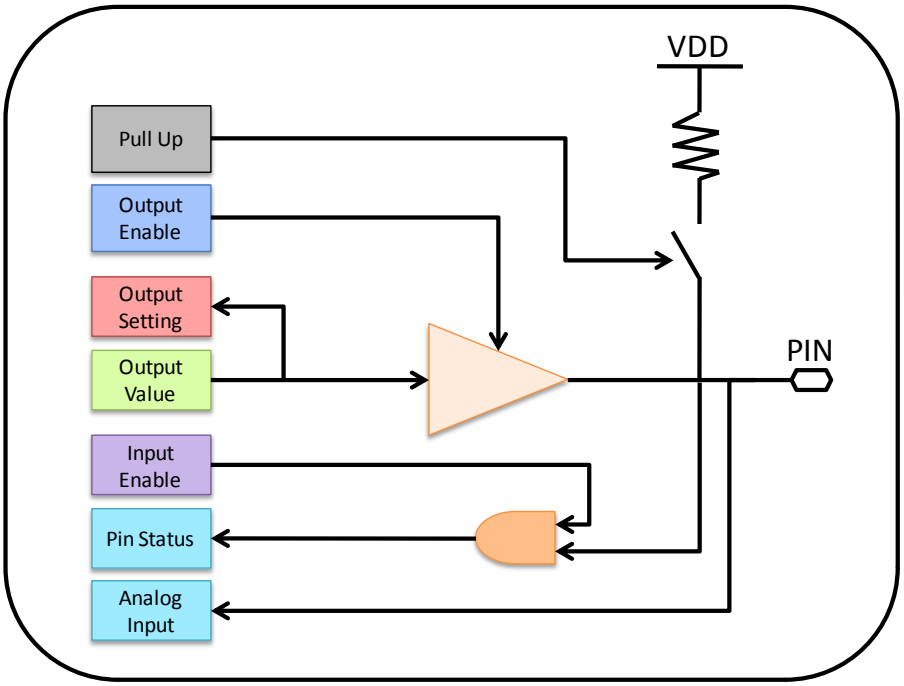


Fig. 11 GPIO Block Diagram

In **Fig. 12 GPIO Interrupt Block Diagram**, the interrupt block diagram shows how GPIO is assigned to the interrupt sources. All GPIO pins support one of the 3 interrupt mode: rising, falling, & dual-edge. CPU wake-up function and debounce @ 1 ~ 128x256 PCLK are also supported.

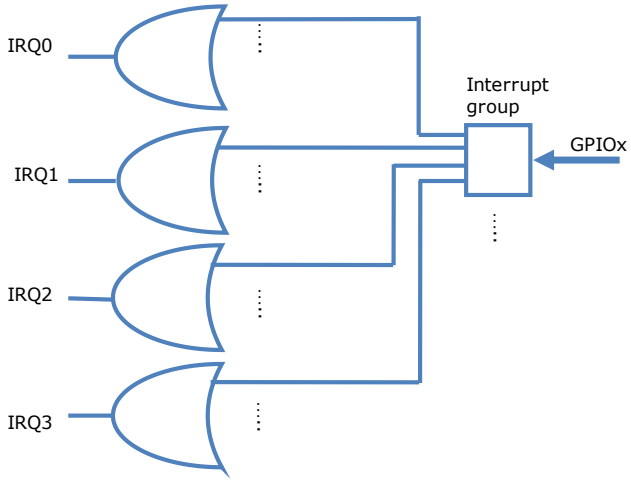


Fig. 12 GPIO Interrupt Block Diagram

7.18 UART

There are two sets of UART with flow control in the controller. One is High Speed UART @ 1Mbps and the other is a Normal Speed UART @ 115.2Kbps.

- 64 byte/16 byte entry FIFOs for received and transmitted data payloads
- Flow control function (CTS, RTS) supported
- Programmable baud-rate generator that allows the internal clock to be divided by 2 to (2^16 + 1) to generate an internal 16X clock.
- Fully programmable serial-interface characteristics:
- 5-, 6-, 7-, or 8-bit character
- Even, odd, or no-parity bit generation and detection
- 1-, 1&1/2, or 2-stop bit generation
- Baud rate generation
- False start bit detection.

7.19 USB (Universal Serial Bus)

The USB2.0 Full Speed device interface:

- Full Speed 12Mbps.
- Provide 1 interrupt source with 4 interrupt events.
- Provide 6 programmable endpoints that support Control, Bulk In/Out, Interrupt and Isochronous transfers.
- Suspend when no bus signaling for 3 ms.
- Include 512-Byte internal SRAM as USB buffer.

Provide remote wakeup capability.

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Rating

Ambient temperature ..... -40°C ~ 105°C

Storage temperature ..... -40°C ~ 125°C

Voltage on any pin ..... -0.3V ~ 3.6V

Power supply voltage (Core logic) ..... -0.5V ~ 2.5V

Power supply voltage (IO Buffer) ..... -0.5V ~ 4.6V

Injection current (latch-up testing) 100mA

Crystal Frequency ..... 2MHz ~ 20MHz

8.2 DC Characteristics

(V_{DD33} = 3.3V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	IO Post-Driver Voltage		3.00	3.30	3.60	V
AO_VREF18	DAC Operation Voltage		1.62	1.8	1.98	V
V_{BAT}	RTC Voltage		1.2	1.5	1.8	V
V_{CORE}	Core Logic, Pre-Driver Voltage		1.62	1.80	1.98	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		3.6	V
V_T	Threshold Point		1.30	1.36	1.42	V
V_{T+}	Schmitt trigger L-to-H threshold point		1.51	1.56	1.60	V
V_{T-}	Schmitt trigger H-to-L threshold point		1.15	1.21	1.25	V
I_{CC}	Supply Current	F_{CPU} = 80MHz			27	mA
I_I	Input Leackage Current	V_I = 3.3V or 0V	-1		1	uA
I_{OZ}	Tri-State Output Leakage Current	V_O = 3.3V or 0V	-1		1	uA
V_{OL}	Output Low Voltage	I_{OL} = 4 / 8 / 12 mA			0.4	V

V_{OH}	Output High Voltage	I_{OL} = 4 / 8 / 12 mA	2.4			V
I_{OL}	Low-Level Output Current, 4mA	V_{OL} = 0.4V	4			mA
	Low-Level Output Current, 8mA	V_{OL} = 0.4V	8			mA
	Low-Level Output Current, 12mA	V_{OL} = 0.4V	12			mA
	Low-Level Output Current, 16mA	V_{OL} = 0.4V	16			mA
I_{OH}	High-Level Output Current, 4 mA	V_{OH} = 2.4V	-4			mA
	High-Level Output Current, 8 mA	V_{OH} = 2.4V	-8			mA
	High-Level Output Current, 12 mA	V_{OH} = 2.4V	-12			mA
	High-Level Output Current, 16mA	V_{OH} = 2.4V	-16			mA
R_{PU}	Pull-up Resistor		38	54	84	KΩ

(V_{DD33} = 3.3V, All IP disable ,Code run from SRAM.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	Supply Current	F_{CPU} = 48MHz			14.5	mA
		F_{CPU} = 72MHz			18	
		F_{CPU} = 81MHz			20	

(V_{DD33} = 3.3V, All IP disable ,Code run from SPI Flash , SPI Flash clock = CPU clock.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	Supply Current	F_{CPU} = 48MHz			9	mA
		F_{CPU} = 72MHz			9.5	
		F_{CPU} = 81MHz			10.5	

8.3 AC Characteristics

8.3.1 Audio DAC Characteristics

Parameter	Min	Typ	Max	Unit
Operating Voltage (AO_VREF18)	1.62	1.8	1.98	V
Maximum Output Voltage Amplitude (R_L = 50 KΩ)		0.86		V_{P-P}
Operating current		1.8		mA
THD + N (R_L = 50 KΩ, f = 1KHz)		0.05		%
SNR		80		dB

8.3.2 ADC Characteristics

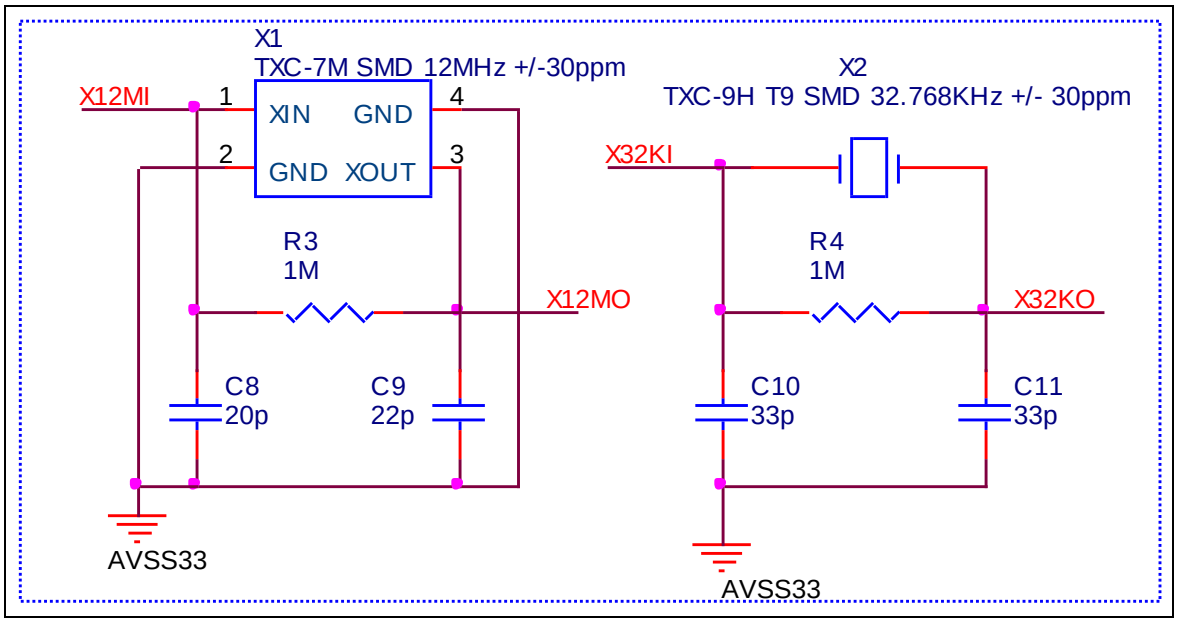
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation voltage	AVDD33		3.0	3.3	3.6	V
Operation Current	I_{DD}			400		uA
Reference voltage	V_{REFP}		2		V_{DD}	V
Reference Current	I_{REFP}	V_{REF} = 3.3V		400		uA
		V_{REF} = 2V		250		uA
Resolution			8	9	10	bit
Conversion time			2.5		10	us
Sampling rate					400K	Hz
Integral Non-Linearity Error	I_{NL}				±2	LSB
Differential Non-Linearity	D_{NL}				±1	LSB

8.3.3 Voice Recorder Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation voltage	V_{DD}		3.0	3.3	3.6	V
Operation Current	I_{DD}			2.4		mA

Sampling rate	SR				16	KSPS
Input Resistance	M_{ICP}			5		KΩ
Input Resistance	M_{ICM}			55		KΩ
THD + N				50		dB
SNR				60		dB

9. TYPICAL APPLICATION CIRCUITS



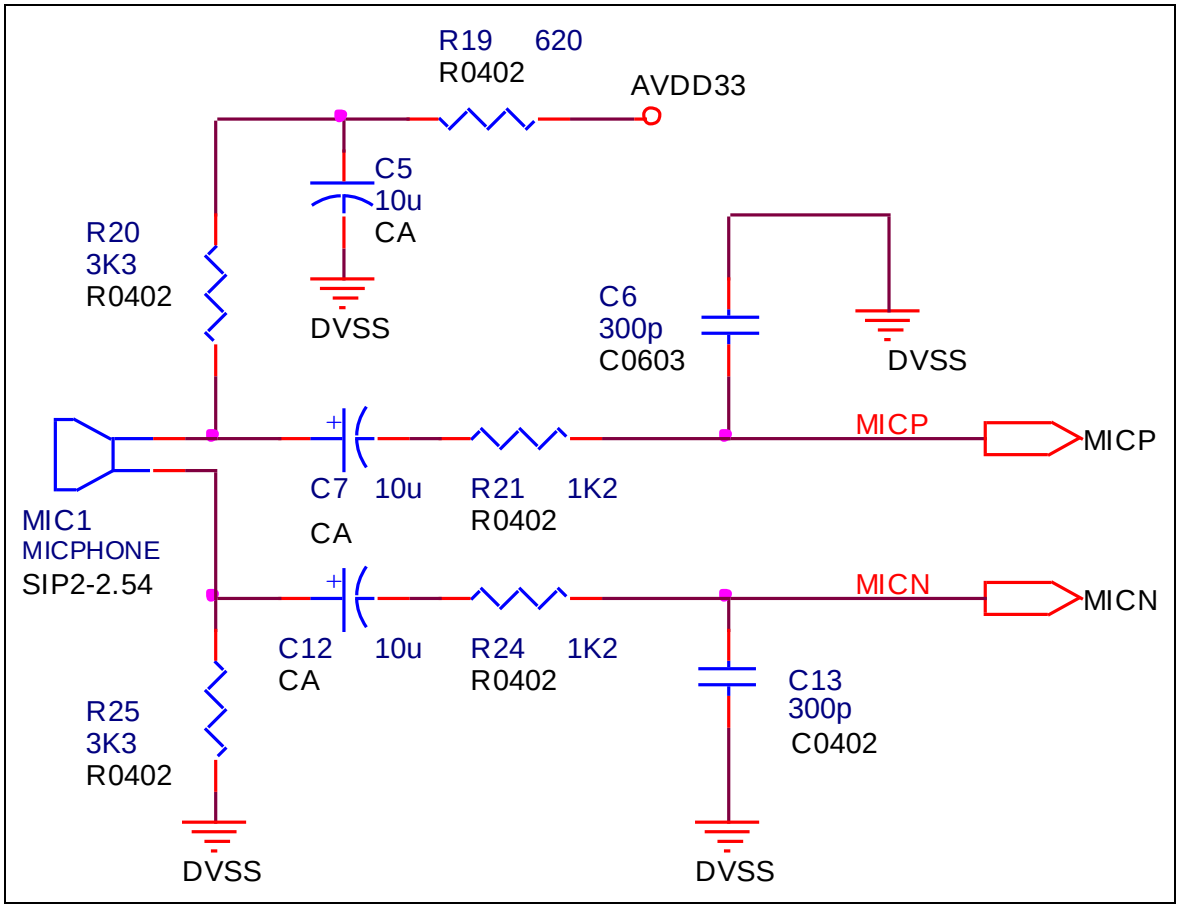
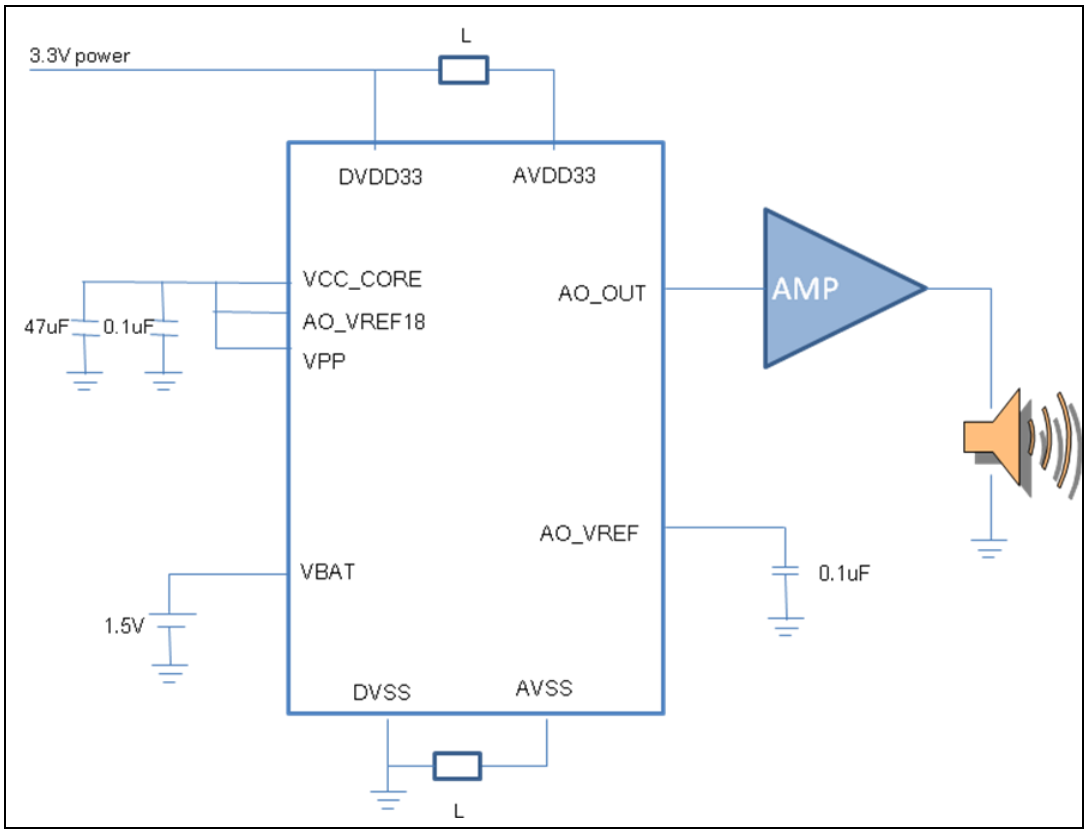


Fig. 13 Connections @ X'tal & MIC



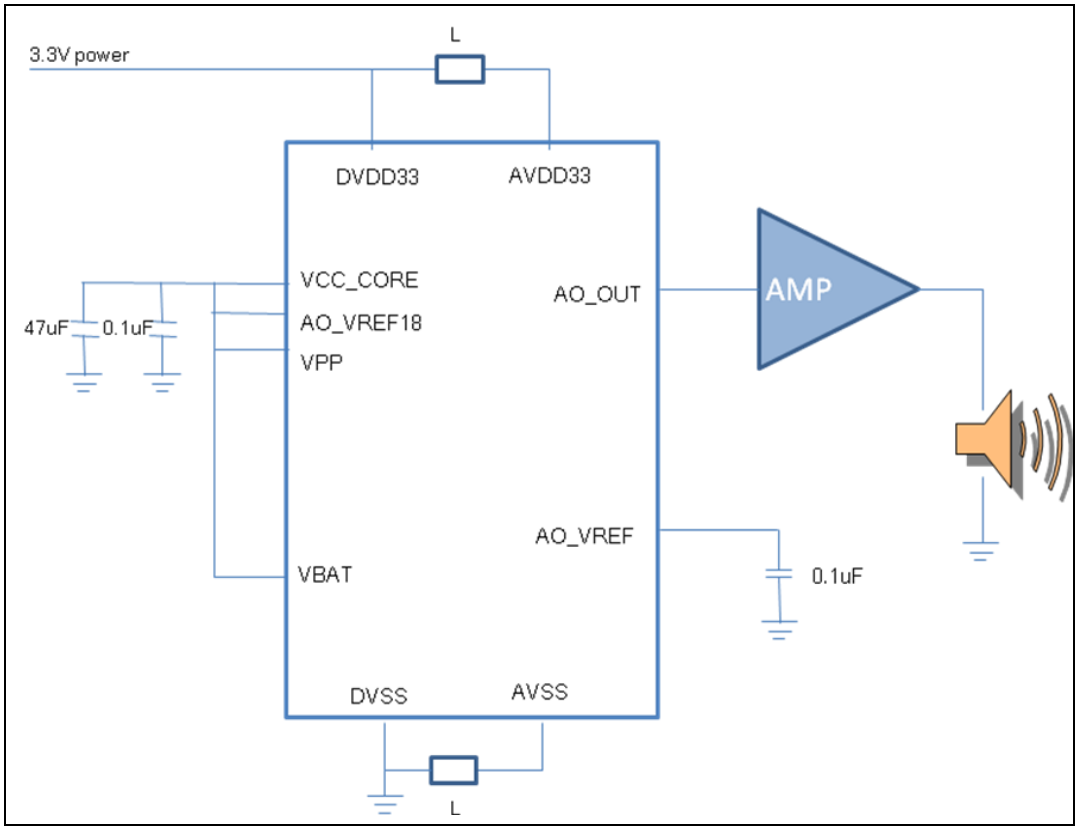


Fig. 14 Connections @ Digital / Analog Power Pins

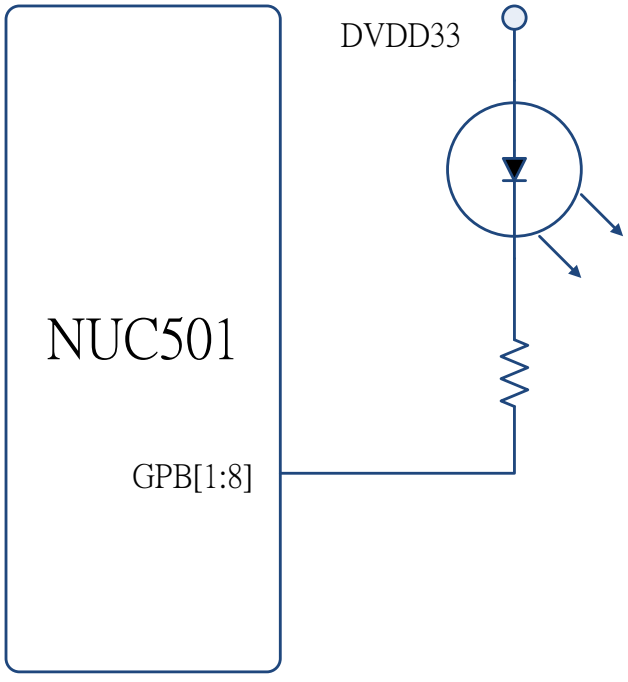
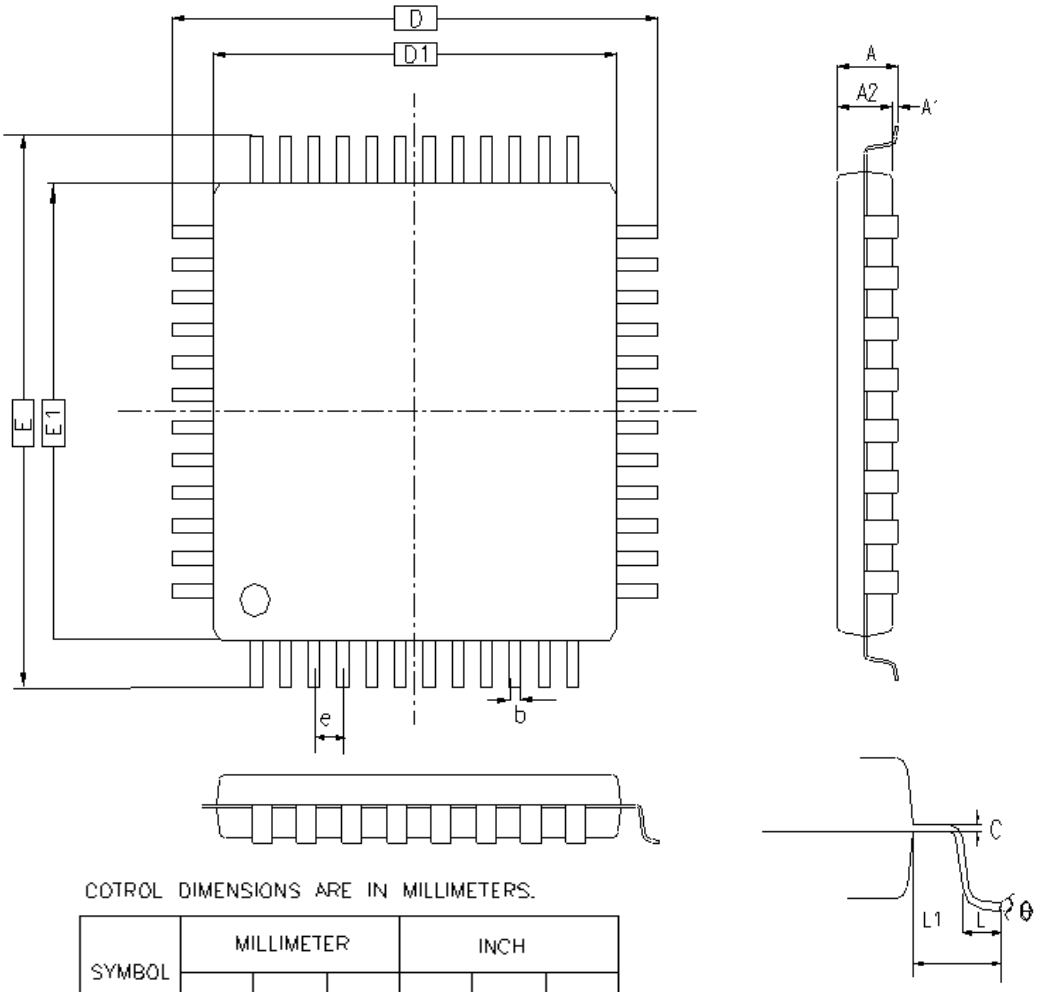


Fig. 15 Direct Sink I/O for LED

10. PACKAGE SPECIFICATION

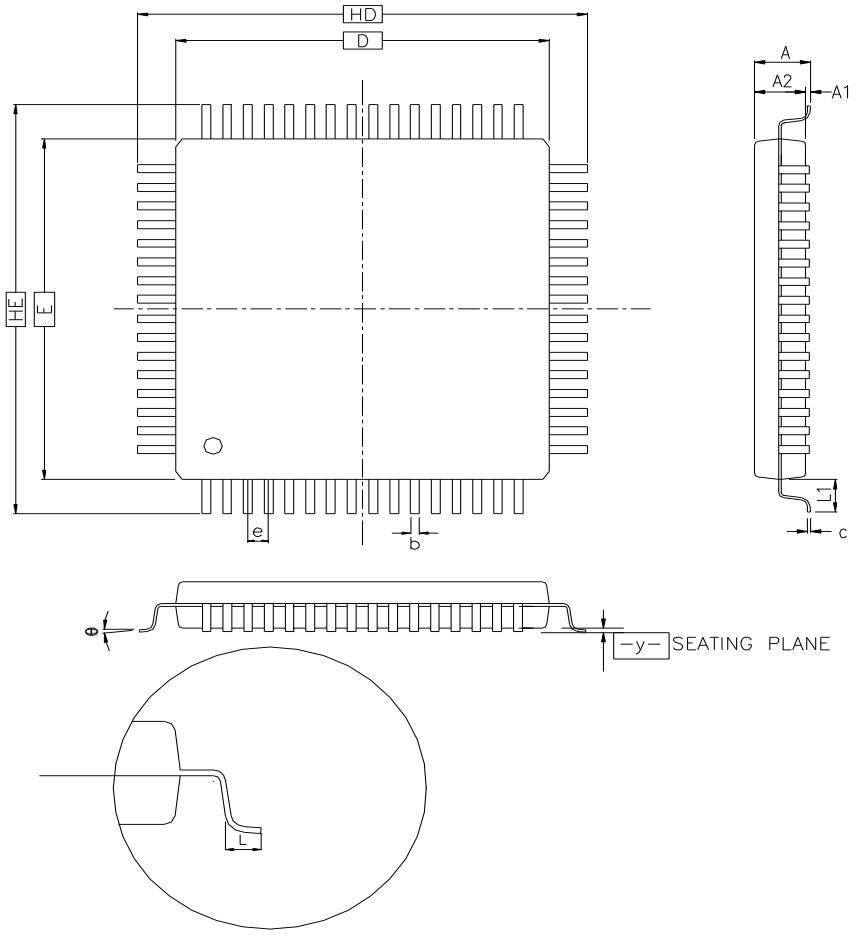
LQFP-48 (7x7x1.4mm footprint 2.0mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.260
E1	6.90	7.00	7.10	0.272	0.276	0.260
e	0.35	0.50	0.65	0.014	0.020	0.260
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

LQFP-64 (10x10x1.4mm)



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.60
A_1	0.05	—	0.15
A_2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	—	0.20
D	—	10.00	—
E	—	10.00	—
e	—	0.50	—
H_D	—	12.00	—
H_E	—	12.00	—
L	0.45	0.60	0.75
L_1	—	1.00	—
y	—	0.10	—
θ	0°	3.5°	7°

11. ORDERING INFORMATION

PART NO.	PACKAGE TYPE	SPECIAL ITEMS
NUC501ADN	48-pin LQFP	RoHS-compliant Green Part
NUC501BDN	64-pin LQFP	RoHS-compliant Green Part

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Feb. 28, 2009	ALL	Initial release.
A1.1	Mar. 20, 2009	ALL	Update diagram font.
A1.2	April. 23, 2009	ALL	Change CPU speed up to 108MHz.
A1.3	April. 30, 2009	33	Update LQFP-48 package specification
A.1.4	May. 21, 2009	16	Add Power on setting table for IBR
A1.5	Sep. 20, 2011	ALL	Change CPU speed to 81MHz Fix the DC specification of I/O

Important Notice

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