October 2015
Revision 1.15

NPCP215F Audio Enhancing Engine and Power Amplifier Family

General Description

The Nuvoton NPCP215F device is a member of Nuvoton's Sound Enhancing family optimized for TV applications.

The NPCP215F integrates a Class-D power amplifier with Waves® MaxxAudio-3 sound enhancement algorithms. These are proprietary, patented, psychoacoustic algorithms that compensate for the acoustic limitations of small-dimensioned consumer electronics devices and speakers.

MaxxAudio-3 algorithms enable reproduction of rich content, with a wide dynamic range and a full frequency range, on a limited audio system. For low-frequency reproduction, MaxxBass® uses a patented psychoacoustic technique to create a perceived low bass, which can be extended up to 1.5 octaves lower than the original. This technique reproduces full and rich sounding bass tones. Power handling is done by MaxxVolume, which utilizes the power amplifiers and speakers to their full extent yet avoids clipping and distortions.

The MaxxAudio-3 software suite provides additional algorithms that enhance the overall sound quality, such as Maxx3D, which widens the stereo image, and MaxxTreble for reproducing crystal clear high frequencies. To design a resonance-free audio system, MaxxEQ provides a flexible equalizer with 20 bands.

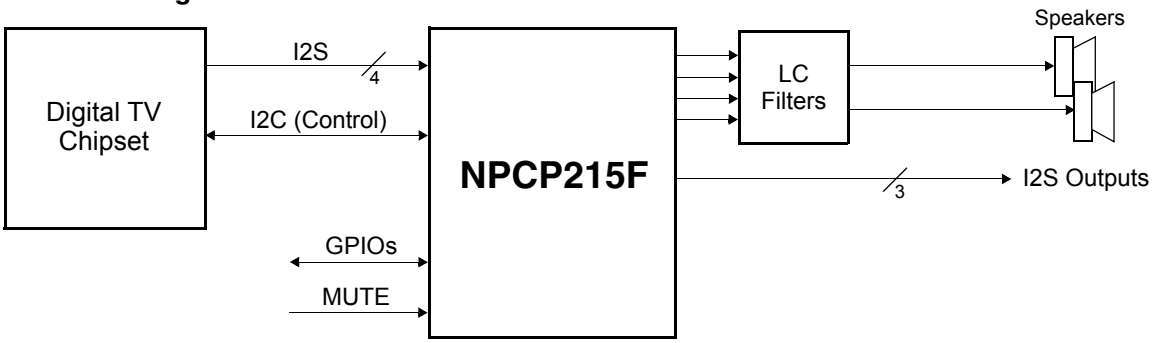
Specifically designed for devices such as TV, MaxxLeveler maintains a constant level of output for any given content. This feature is useful for maintaining the same volume during commercials or when switching TV channels.

The MaxxAudio Graphical User Interface (GUI) enables sound engineers to easily tune the device and customize presettings for different audio products.

Outstanding Features

- Improves audio quality for low-performance speakers
- System-level BOM savings
- I2C controlled
- 24-bit accuracy
- Audio algorithms
  - MAXXBASS®
  - MAXX3D
  - MAXXTREBLE
  - MAXXEQ
  - MAXXVOLUME®
  - MAXXLEVELER
  - MAXXDIALOG
- Audio input: up to four I2S or Synchronous Serial Interface (SSI) inputs
- Audio output:
  - Up to three I2S or SSI outputs
  - Class-D Power output up to 2 x 20W
- 100 dB SNR
- Typical power efficiency of 90%
- Various protection sensors
- Several General-Purpose digital signals available to the application (GPIOs)
- Logic supply of 3.3V and Power supply up to 26.4V
- 7 x 7 mm, 48-pin Quad Flat No-Lead (QFN) package

System Block Diagram



Features

Bus Interfaces

- Synchronous Serial Interface (SSI)
  - Compatible with I2S
- I2C Interface
  - Compliant with *I2C-BUS Specification Revision 1.0, 1992*
  - Master or slave interface
  - Supports 7-bit address mode

Audio Enhancing Engine

- Processing Unit
  - 24-bit
  - 125 MIPs

Audio Algorithms

- MaxxBass®
  - Patented Waves MaxxBass psycho-acoustic bass extension delivers a more natural sound than traditional bass boost technologies, which use EQ and can overpower your system. MaxxBass analyzes low frequencies to create harmonics that are perceived as lower, deeper tones.
- Maxx3D
  - Maxx3D extends the span of stereo-side content while maintaining the integrity of unprocessed center content.
  - Maxx3D improves the stereo separation of speakers, widening the stereo field for optimal imaging.
- MaxxTreble
  - MaxxTreble delivers crystal clear high-frequency enhancement for increased RMS without exceeding the system ceiling. Its proprietary algorithm restores luster to over-compressed formats to provide the perfect listening experience.
- MaxxEQ
  - MaxxEQ provides the ability to design EQ curves and shape sound with surgical precision, using up to 20 programmable filters with bell, shelf, low pass, and high pass, plus adjustable frequency, gain, and Q parameters. MaxxEQ's intuitive Graphic User Interface makes click-and-drag filter design fast and easy.
- MaxxVolume®
  - MaxxVolume is an all-in-one volume control, with High-Level Compression to increase RMS levels, Low-Level Compression to increase the clarity of soft sounds, Noise Gating to eliminate signal and system noise, and Leveling to smooth out volume levels.

    It includes:
    - Leveler - (replaces traditional AGC)
    - Low-level gain
    - Dynamic range curve controller
    - Noise gate
- MaxxLeveler
  - MaxxLeveler regulates the perceived volume of the audio, keeping all audio content at the same level.
- MaxxDialog
  - MaxxDialog is a revolutionary new technology that enables users to adjust center channel dialog levels without affecting the rest of the audio mix. Based on the Waves Center pro audio plug-in, MaxxDialog delivers clear, crisp dialog that does not disappear behind loud music and effects.
- Sub-Woofer
  - Enables separating low-frequency content and directing it into a third audio channel, for driving a subwoofer.

Power Amplifier

- Class-D Power up to 2 x 20W to 6 Ω or 8 Ω (0.5% THD)
- Typical power efficiency of 90%
- 100 dB SNR
- Less than 0.4% THD at 1W
- Protection:
  - Over-current
  - Under-voltage
  - Over-temperature

Straps, Clocks, Supply and Package Information

- Strap Input Controlled Operating Modes
  - PLL reference clock select (REF strap)
  - Test mode select (nTEST strap)
  - I2C master or slave select (I2CMS strap)
  - Boot options
    - ROM code operation
    - Loadable algorithms for new functions or ROM code patching
- Input Clocks
  - SSI / I2S clock: 1 MHz - 5 MHz input
  - Optional crystal oscillator or input clock
- Power Supply
  - 3.3V Logic supply
  - 9V to 26.4V Power supply
- Power-Save Modes
  - Power-down of less than100 mW
  - Power stage shut down
- Package
  - 7 x 7 mm, 48-pin Quad Flat No-Lead (QFN) package

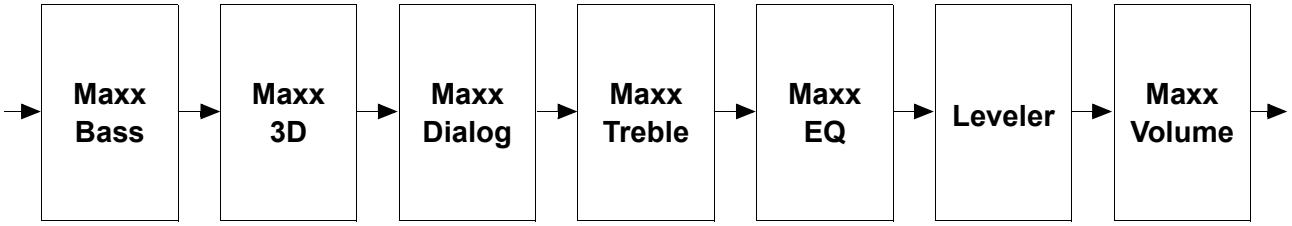
Features (Continued)

Derivative Table

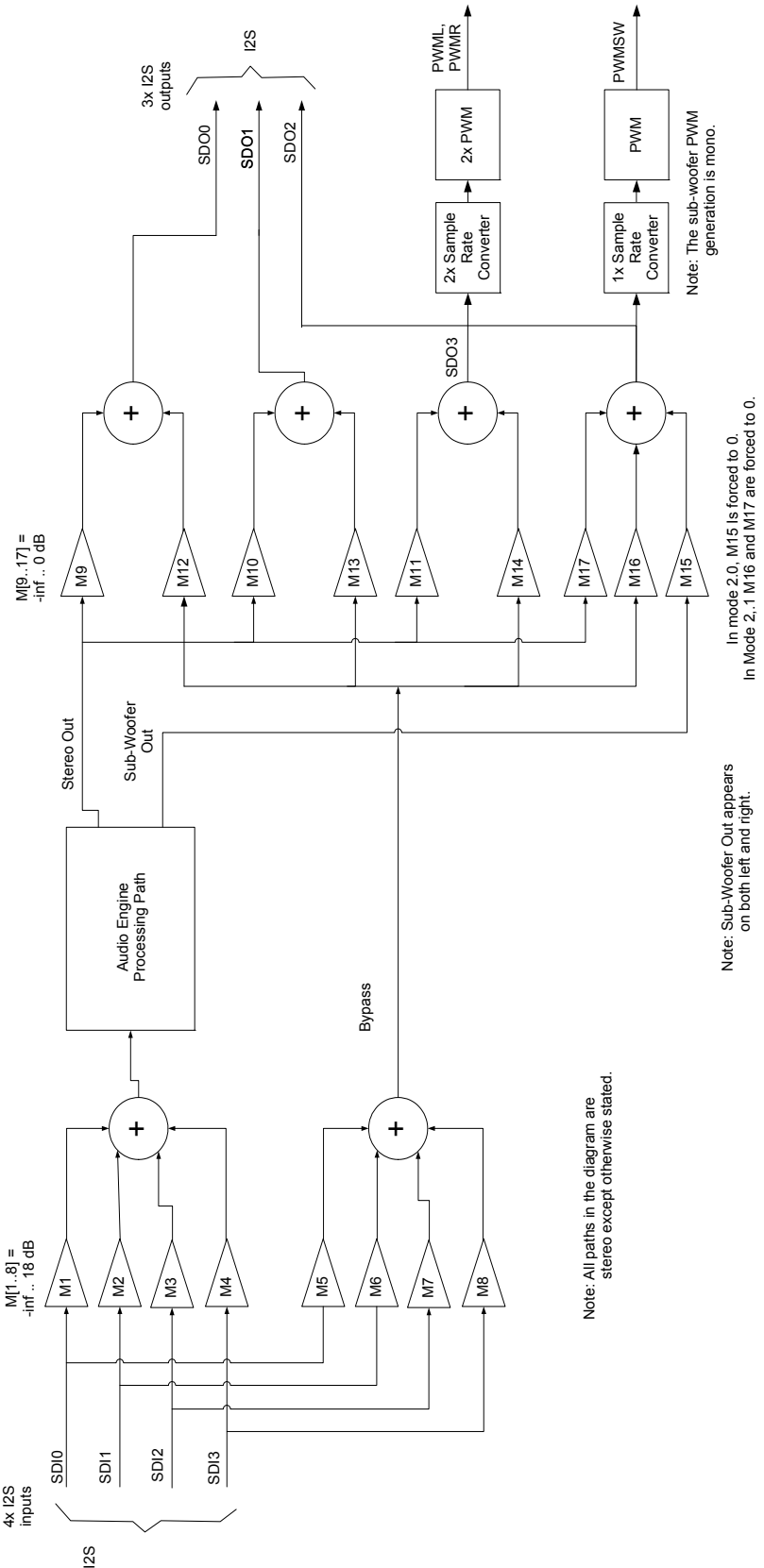
Product	ID[1]	Package	I2S Stereo Inputs	Output Power	Algorithms						
					Maxx Bass	Maxx EQ	Maxx Treble	Maxx Volume	Maxx Leveler	Maxx 3D & Maxx Dialog	Sub-Woofer Support
NPCP215F	0011	QFN48	4	2x20W	◆	◆	◆	◆	◆	◆	◆

1. Includes 4 bits: Bits 3-1 are the DEVSEL field, bit 0 is the ALLALGEN bit.

Algorithm Processing Chain



Features (Continued)



Device Audio Path Block Diagram

Revision Record

Date	Status	Comments
July 2013	Revision 0.9	Datasheet first revision.
August 2013	Revision 1.0	Updated max operating voltage to 26.4V.
November 2013	Revision 1.1	• Corrected drive levels of EVNT and CLKOUT signals. • Updated 2.1 channel description. • Updated table in Section 4.1.4.
October 2015	Revision 1.15	• Added Integration block diagram (Section 3.1). • Removed 2.1 channel support. • Removed NPCP215B version. • Removed Single-Ended functionality.

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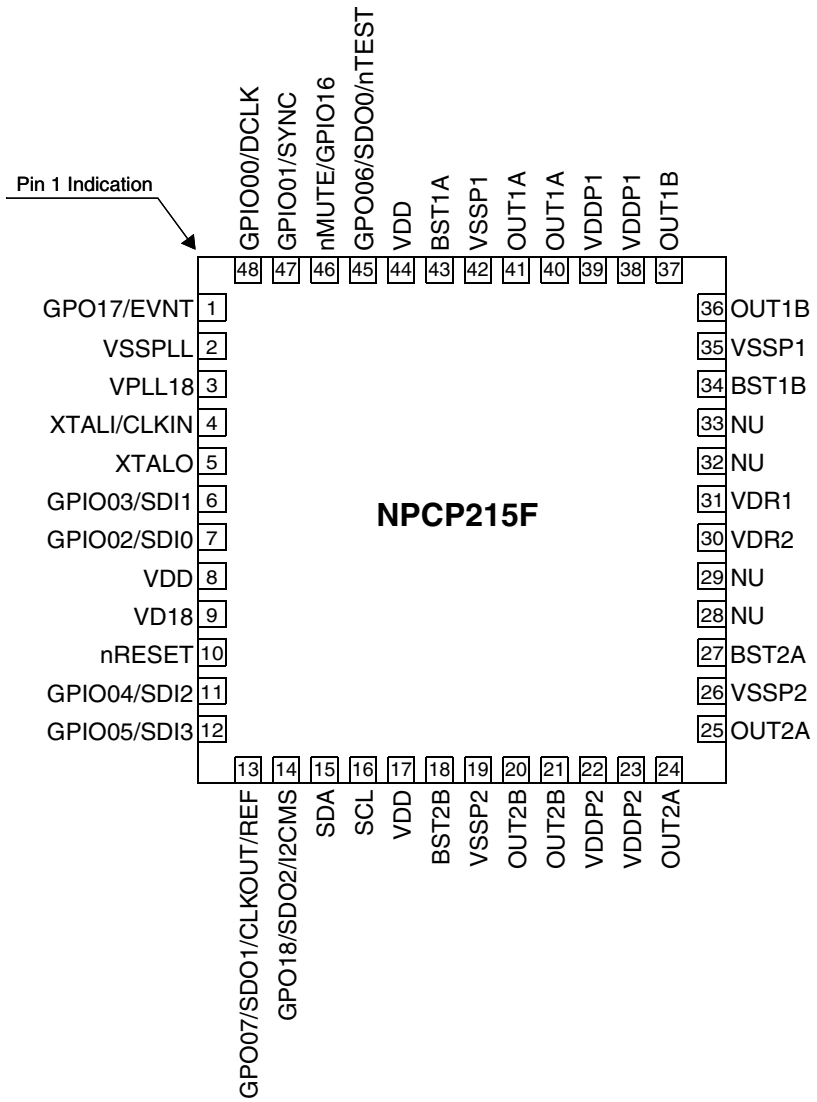
1.0 Signal/Pin Description

1.1 CONNECTION DIAGRAM



Note: Bottom Pad is VSS (must be connected to digital ground)

48-Pin Quad Flat No-Lead (QFN) Package
Order Number: NPCP215FA0YX

1.0 Signal/Pin Description (Continued)

1.2 PIN TYPES

Table 1. Abbreviations

Abbreviations	Description
GPIO	General-Purpose Input/Output
GPO	General-Purpose Output
GPI	General-Purpose Input
Ox/y	Output, Source x mA, Sink y mA
ODy	Output, Open-Drain, Sink y mA
5V	Input tolerant to 5 volts
PU	Input buffer with a pull-up resistor. This pull-up resistor is intended to maintain unconnected input pins at high logic level. The voltage measured externally on an unconnected input pin is in the range of 1.5 to 2.5V, although the input itself is near V_{DD} level.
T	Input buffer with CMOS / LVTTL levels
ST	Schmitt trigger input buffer with CMOS / LVTTL levels
A	Analog input or output
XO	Crystal Oscillator

1.3 PIN DESCRIPTION

1.3.1 Clocks and Reset

Note: Crystal oscillator connections are found in Figure 4 on page 15.

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
XTALI/CLKIN	I	**Crystal Clock Input**. Used for a crystal connection circuit or as a clock input (clock input at LVTTL levels). The crystal should have a frequency of 12.288 MHz or 11.2896 MHz.		VDD	XO	
XTALO	O	**Crystal Clock Output.** Used for a crystal connection circuit.				
nRESET	I	**Power-Up Reset Input.** If driven low, forces reset. This input has a filter and ignores pulses of less than 5 ns.	PU	VDD	5V, ST	

1.0 Signal/Pin Description (Continued)

1.3.2 GPIO/ Other

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
GPO17 / EVNT	O O	**General-Purpose Output Signal 17. /** **Event Indication.** May be used as an interrupt signal to the system controller.	PU	VDD	O6/6	
nMUTE / GPIO16	I I/O	**Mute Output.** Mutes output level when pulled low. May be left open if not used. / **General-Purpose I/O Signal 16.**	PU	VDD	ST,5V,O2/2	

1.3.3 I2S / GPIO / STRAPS

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
GPIO00 / DCLK	I/O I/O	**General-Purpose I/O Signal 00.** / **I2S Clock.** Input for an I2S slave and output for an I2S master. The frequency must be either 32 or 64 times the sample frequency. When used as output, a 33Ω to 100Ω series resistor is required.	PU	VDD	T,5V,O2/2	
GPIO01 / SYNC	I/O I/O	**General-Purpose I/O Signal 01.** / **I2S SYNC.** Input for an I2S slave and output for an I2S master. Indicates the sample frequency. When used as output, a 33Ω to 100Ω series resistor is required.	PU	VDD	T,5V,O2/2	
GPIO02 / SDI0	I/O I	**General-Purpose I/O Signal 02.** / **I2S Serial Data In 0.** Carries input stereo data stream 0.	PU	VDD	T,5V,O2/2	
GPIO03 / SDI1	I/O I	**General-Purpose I/O Signal 03.** / **I2S Serial Data In 1.** Carries input stereo data stream 1.	PU	VDD	T, 5V, O2/2	
GPIO04 / SDI2	I/O I	**General-Purpose I/O Signal 04.** / **I2S Serial Data In 2.** Carries input stereo data stream 2.	PU	VDD	T,5V,O2/2	
GPIO05 / SDI3	I/O I	**General-Purpose I/O Signal 04.** / **I2S Serial Data In 2.** Carries input stereo data stream 2.	PU	VDD	T,5V,O2/2	
GPO06 / SDO0 / nTEST	O O I	**General-Purpose Output Signal 06.** / **I2S Serial Data Out 0.** Carries output stereo data stream 0. A 33Ω to 100Ω series resistor is required. / **Test Strap.** Sampled during Power-Up reset. The pin is pulled up by an internal resistor for normal operation or set to 0 by an external 8.2 KΩ pull-down resistor.	PU	VDD	T,5V,O2/2	

1.0 Signal/Pin Description (Continued)

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
GPO07 / SDO1 / CLKOUT / REF	O O O I	**General-Purpose Output Signal 07.** / **I2S Serial Data Out 1.** Carries output stereo data stream 1. A 33 to 100 Ω series resistor is required. / **General-Purpose Clock Output.** A 33Ω to 100Ω series resistor is required. / **Reference Strap.** Sampled during Power-Up reset. The pin is pulled up by an internal resistor (selects DCLK in) or set to 0 by an external 8.2 KΩ pull-down resistor (selects crystal oscillator).	PU	VDD	T,5V,O6/6	
SDO2 / GPO18 / I2CMS	O O I	**I2S Serial data out 1.** Carries output stereo data stream 2. A 33 to 100 Ω series resistor is required. / **General-Purpose Output Signal 18.** / **I2S Master/Slave Strap.** Sampled during Power-Up reset. The pin is pulled up by an internal resistor (selects slave) or set to 0 by an external 8.2 KΩ pull-down resistor (selects master).	PU	VDD	T,5V,O2/2	

1.3.4 I2C

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
SDA	I/O	**Master/Slave I2C Data Line.** When used as an input, ignores short pulses of a length of less than 5 ns (reducing signal reflections hazards).		VDD	ST,5V,OD6	
SCL	I/O	**Master/Slave I2C Clock Line.** When used as an input, ignores short pulses of a length of less than 5 ns and rejects more signal changes within 20 ns (reducing signal reflections hazards).		VDD	ST,5V,OD6	

1.0 Signal/Pin Description (Continued)

1.3.5 Power Amplifier

See recommended connection in Figure 5 on page 16.

Signal	I/O	Description	Pull-Up / Down	Power Well	Buffer Type	Comments
OUT1A, OUT1B, OUT2A, OUT2B	O	**Power Stage Output.** These outputs each use 2 pins that must be connected together. They should be connected via an LC filter to speakers.		VDDP	Power	
BST1A, BST1B, BST2A, BST2B	A	**Bootstrap Connection.** These pins must each be connected via a 100 nF ceramic capacitor to the respective power output pin (OUT1A, OUT1B, OUT2A or OUT2B).		VDDP	Analog	
VDR1, VDR2	A	**Regulator Filter.** These pins must each be connected via a 1μF ceramic capacitor to power ground.		VDDP	Analog	
VDDP1, VDDP2	A	**Supply for Power Amplifier.** These signals each use 2 pins that must be connected together to a supply of 9-26.4V.		VDDP	Analog	
VSSP1, VSSP2	A	**Ground for Power Amplifier.** These signals must be connected together to power ground. The Power Amplifier ground must be connected to the digital ground near the device.		VDDP	Analog	

1.3.6 Power

Signal	I/O	Description
VSSPLL	G	**PLL Ground.** PLL ground supply connection. Should be connected to digital ground.
VPLL18	P	**PLL 1.8V Supply.** Internally generated for PLL. Should be connected via a 4.7 μF ceramic capacitor to VSSPLL.
VD18	P	**Internal 1.8V Supply.** Internally generated for internal logic. Should be connected via a 4.7 μF ceramic capacitor to digital ground.
VSS	G	**Digital Ground.** Should be connected to a digital ground plane. The package bottom pad must be connected to digital ground.
VDD	P	**3.3V Digital Supply.**

1.3.7 Not Connected

Signal	I/O	Description
NC		**Not Connected.** Should be left open and not be connected to any signal.

2.0 Power, Clocks and Reset

2.1 POWER

2.1.1 Power Planes

The NPCP215F has two power plane groups (wells), as shown in Table 2.

Table 2. NPCP215F Power Planes

Power Plane Group	Description	Power Plane Notation	Power Pins	Ground Pins
Internal group	Powers the internal logic of all the device modules and PLLs. Supply is generated internally but requires a filtering capacitor.	V_{D18}	VD18, VPLL18	VSS, VSSPLL
Active group	3.3V power to the I/O interface and internal regulators.	V_{DD}	VDD	VSS

2.1.2 Power States

The NPCP215F has the following main power states:

- **Power Fail**
  All power planes are powered off (V_{DD} is inactive).
- **Power Active**
  All power planes are powered on (V_{DD} is active).

2.1.3 Power Connection and Layout Guidelines

The NPCP215F requires a power supply voltage of 3.13V–3.47V for V_{DD}.

V_{DD} uses a common ground return named “Digital Ground” and marked V_{SS}.

The following directives are recommended for the NPCP215F power and ground connections.

Ground Connection

Use a ground plane for digital signals (VSS). Make the following ground connections:

- Connect all VSS pins and the bottom pad of the NPCP215F to the GND plane.
- Connect all VSSP1-2 pins to a plane with the power amplifier components and connect this plane to the GND plane near the NPCP215F device.
- Locate the decoupling capacitors of the Active power plane’s digital supply (VDD) pins close to a VDD pin; connect one terminal of each capacitor to the ground plane.
- If there is insufficient room for decoupling capacitors, place smaller capacitors close to the power-ground pins and larger capacitors further away.

Note that low-impedance ground layers improve noise isolation and reduce ground bounce problems.

Power-Up Sequence

The power-up sequence for the NPCP215F is:

- VDD pins rise at the same time and reach a valid level while nRESET is logic low.
- VDDP1-2 rise at the same time and reach a valid level, 0 to 20 ms later.
- nRESET rises to high logic level.

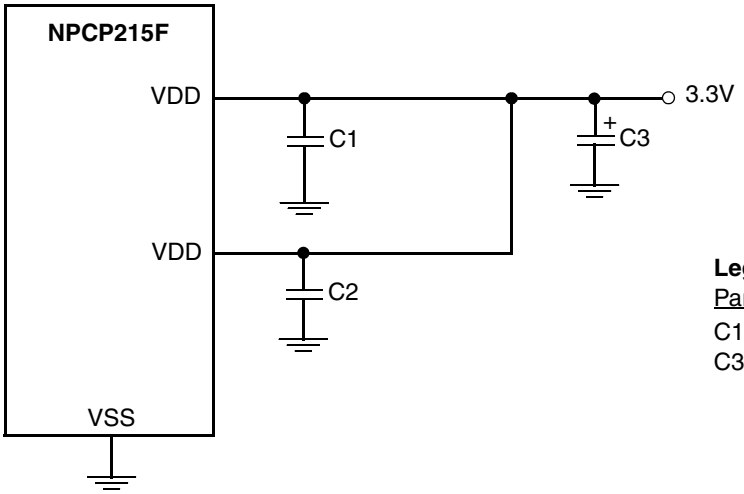
Note: nMUTE may rise to high level at any stage after VDDP is supplied.

2.0 Power, Clocks and Reset (Continued)

2.2 RECOMMENDED SYSTEM CONNECTIONS

All NPCP215F supply pins must be connected to the appropriate power plane. Decoupling capacitors must be used as recommended as follows:

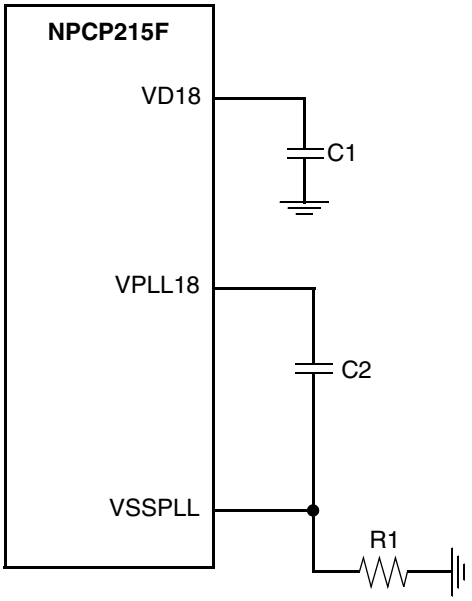
Connect the digital supply pins (VDD) to a 3.3V power supply. A 10 μF (or larger) capacitor should be connected between VDD and the digital ground plane. A 0.1μF capacitor should be connected to ground near each VDD pin of the device. The recommended 3.3 power connections are shown below:



Legend:

Part Designator	Value
C1, C2	0.1 μF Ceramic
C3	10 μF (for linear regulator), 22 μF (for switching regulator)

Figure 1. 3.3V Digital Power Connection Diagram

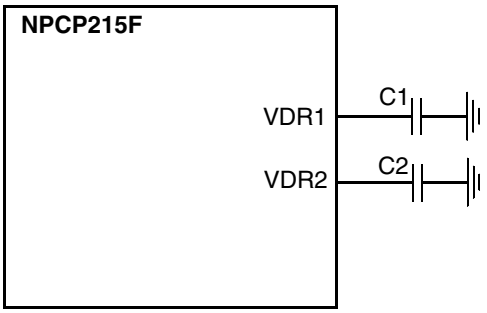


Legend:

Part Designator	Value
R1	0Ω
C1, C2	4.7 μF Ceramic

Figure 2. 1.8V (internal) Power Connection Diagram

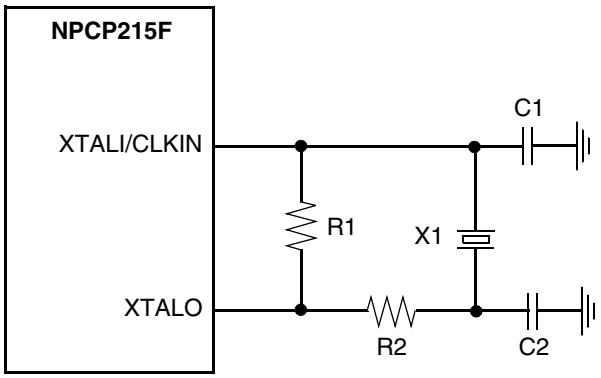
2.0 Power, Clocks and Reset (Continued)



Legend:

Part Designator	Value
C1, C2	1 µF Ceramic

Figure 3. Amplifier Regulator Filters Connection Diagram



Legend:

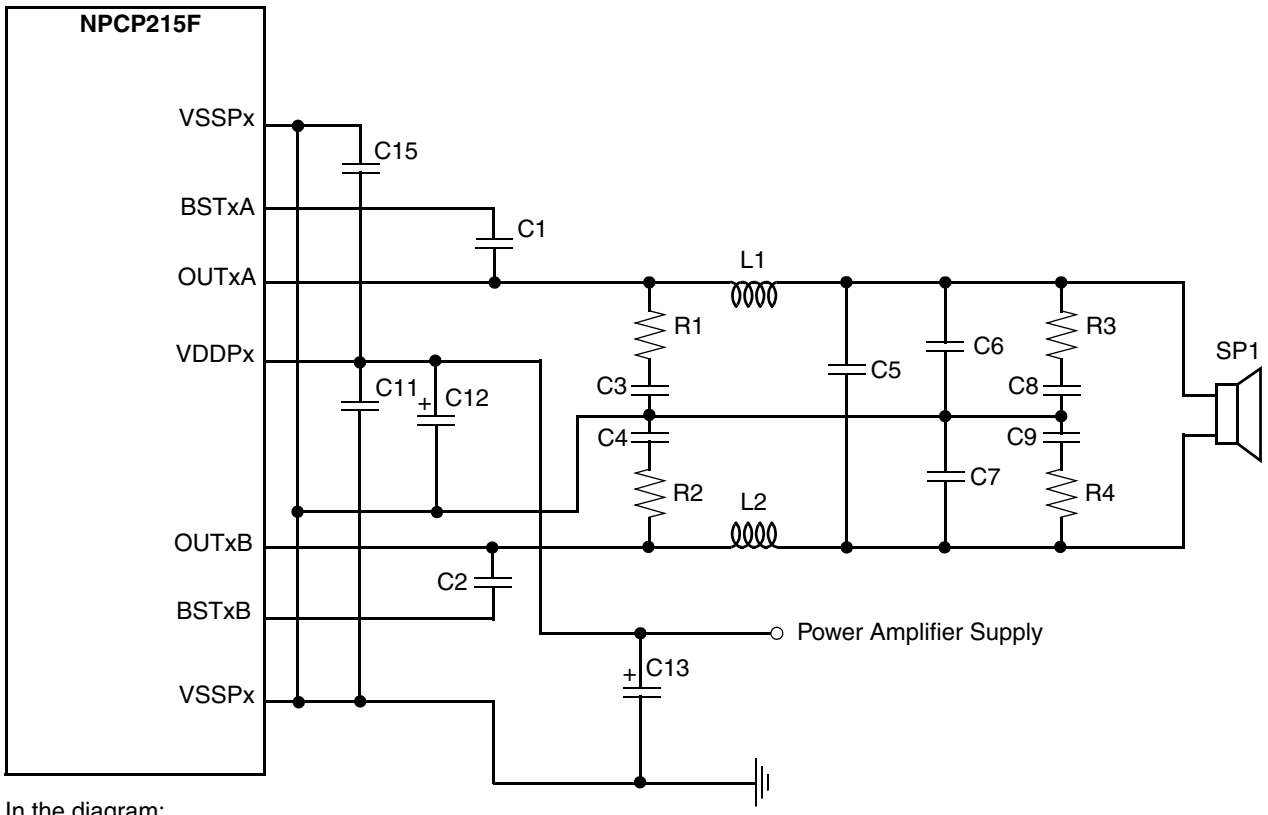
Part Designator	Final Values
R1	2 MΩ 5%,
R2	2000Ω 1%,
C1	20 pF Ceramic 5%,
C2	20 pF Ceramic 5%,
X1	12.288 or 11.2896 MHz, C_L=12 pF, ESR < 75Ω, Drive level up to 500 µW
Alternate values:	
R2	4990Ω 1%,
X1	12.288 or 11.2896 MHz, 100 ppm C_L=12 pF, ESR < 75Ω, Drive level up to 100 µW

Figure 4. Typical Crystal Oscillator Connection Diagram

2.0 Power, Clocks and Reset (Continued)

Board Layout Consideration on Power Amplifier Output:

- The power amplifier supply connections carry high current and must be laid out carefully to reduce EMI generation.
- The bottom plate of the device package must be soldered to a metal plate on the PCB component side.
- The metal plate should have 36 vias connected to a metal plate on the PCB solder side and to the ground plane of the PCB.
- The vias should be filled with solder to provide better thermal conductivity.



In the diagram:
x may be 1 or 2

Connect all power ground connections in a path separate from digital ground.
There should be One connection between power ground and digital ground.

Legend:

Part Designator	Value
C1, C2,	0.1 µF Ceramic, 50V
C3, C4	390 pF Ceramic, 50V
C5	UM
C6, C7	1 µF Ceramic, 50V
C8, C9	Unmounted (UM)
C11, C15	0.1 µF Ceramic, 50V
C12	330 µF, 50V
C13	UM
R1, R2	3.3Ω
R3, R4	UM
L1, L2	22 µH @ 4.5A
SP1	6Ω or 8Ω, 20W

Figure 5. Amplifier Output and Supply Connection Diagram for a Bridge Configuration

2.0 Power, Clocks and Reset (Continued)

2.3 CLOCKS

The NPCP215F clock structure is shown below. The clock generation parameters are supplied to the device at initialization.

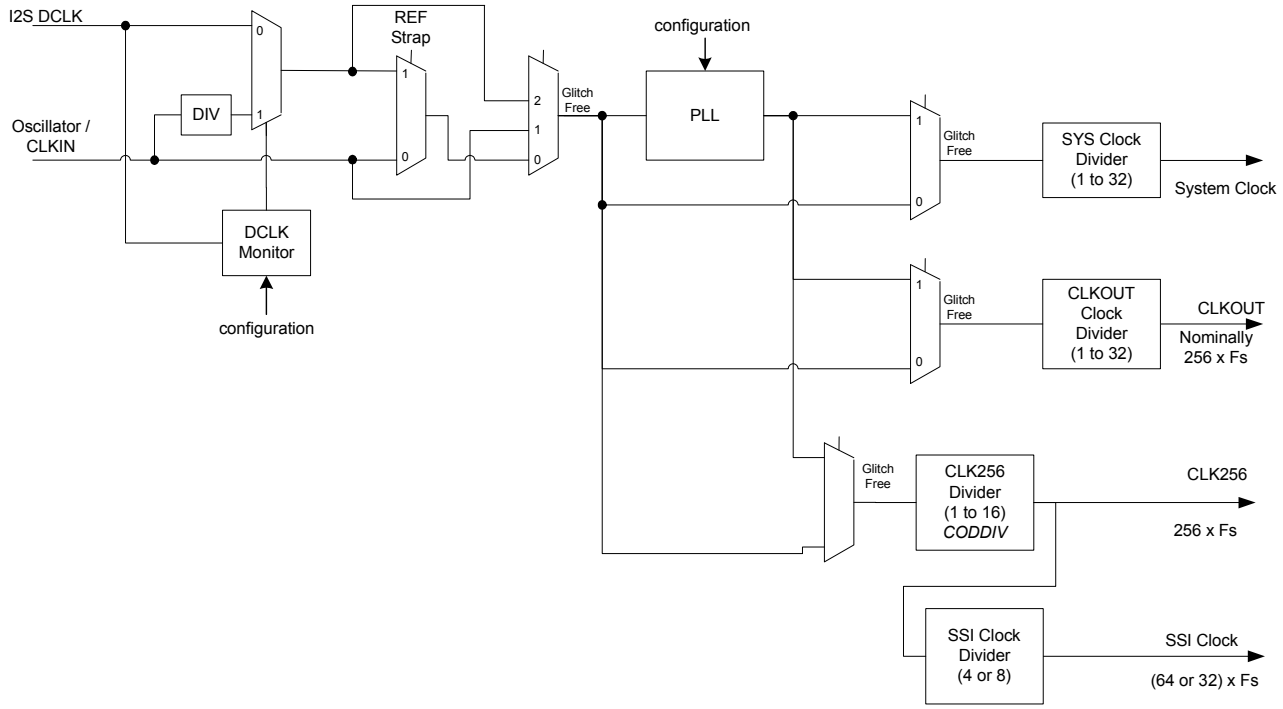


Figure 6. Clocks in the NPCP215F

Clock Source

The clock source is either DCLK (I2S serial clock, in Slave mode) or the crystal oscillator, and is used as the reference clock of the PLL. The clock is selected initially by the REF strap and may be changed later.

When DCLK is a stable clock, the oscillator may be omitted. The oscillator may be replaced by a clock input. DCLK monitoring and SYNC frequency measurement are possible only if an oscillator or clock input are present on the XOSCI/CLKIN pin.

The best selection for a crystal frequency is 256 times the used sample clock.

DCLK Monitoring

When DCLK is used as the PLL reference clock, the DCLK clock monitoring block may be used.

If the monitoring is enabled, and DCLK is selected as the PLL reference clock and also DCLK input is stuck for a programmable time, the PLL reference clock is switched to a clock based on (divided from) the oscillator clock (or CLKIN).

The device supports various sample frequencies. A counter monitors SYNC frequency to enable the firmware to detect any frequency change.

PLL

The PLL is used to generate the system clock and can be used to generate the SSI (I2S) clock as well (if the device is in I2S master mode).

The PLL reference clock may be as low as 44.1 KHz; however, for low jitter, a higher frequency reference clock is recommended.

2.0 Power, Clocks and Reset (Continued)

2.4 RESET SOURCES AND TYPES

The NPCP215F has one reset domain.

Reset Types

- Power-Up reset - Activated when nReset signal is asserted (when the V_{DD} supply is powered up).
- Watchdog reset - Activated when a watchdog condition is detected.

The following sections describe the sources and effects of the various resets on the NPCP215F, per reset type.

2.4.1 Power-Up Reset

V_{DD} Power-Up reset is generated when an nRESET signal is asserted.

On Power-Up reset, the NPCP215F performs the following:

- Puts pins with strap options into TRI-STATE mode and enables the internal pull-up/down resistors on the strap pins
- Samples the values of the strap pins (after nRESET deassertion)
- Performs all actions done by a Watchdog reset

Note: The internal reset signal is active for at least 3 ms.

2.4.2 Watchdog Reset

Watchdog reset is generated by the Watchdog module on detection of a watchdog event.

The NPCP215F loads default values to all registers.

3.0 INTEGRATION

3.1 BLOCK DIAGRAM

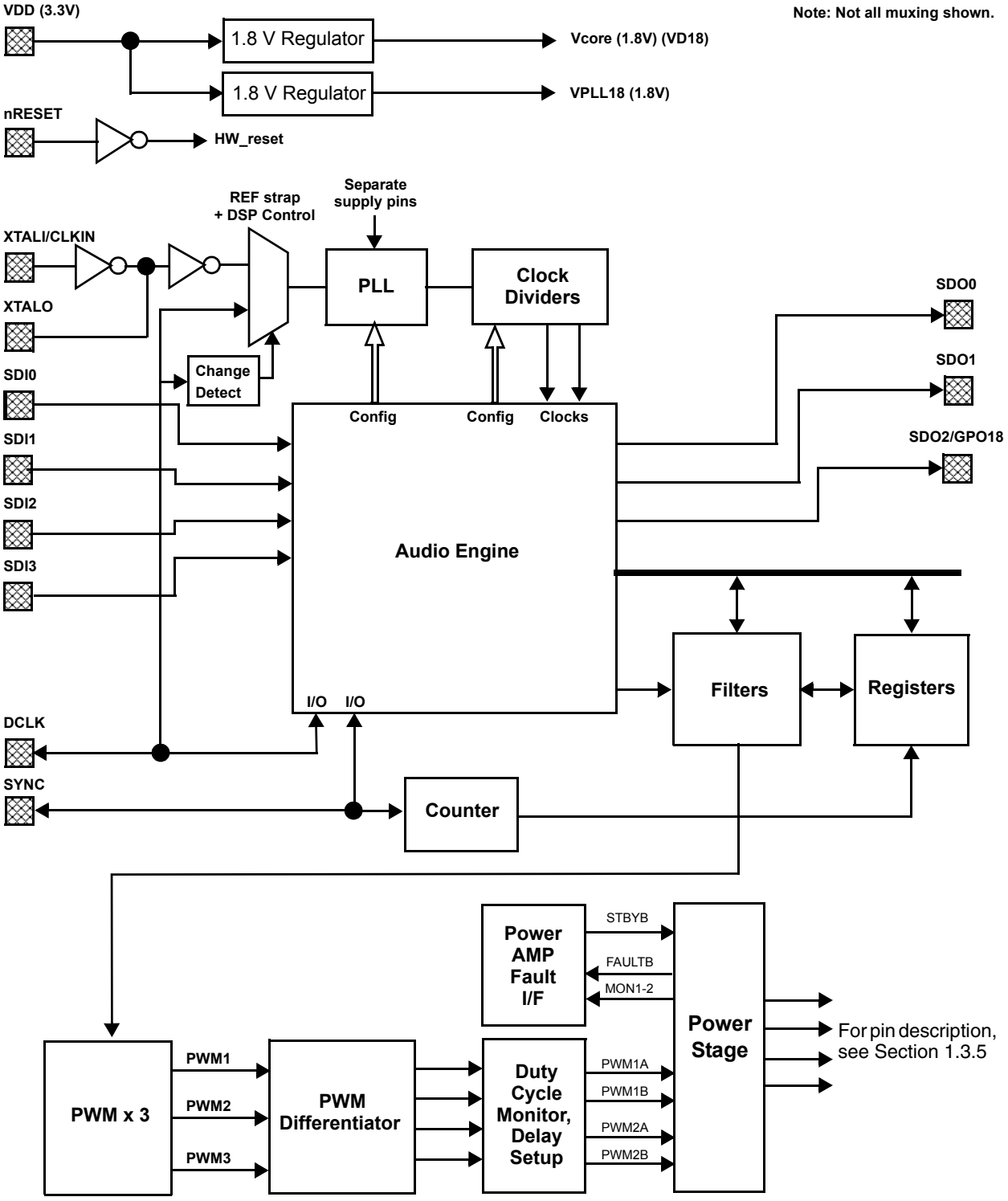


Figure 7. Device Block Diagram

4.0 Device Specifications

4.1 GENERAL DC ELECTRICAL CHARACTERISTICS

4.1.1 Recommended Operating Conditions

Symbol	Parameter[1]	Min	Typ	Max	Unit
V_{DD}	3.3V Supply Voltage (VDD pins)	3.13	3.3	3.47	V
V_{DDP}	Power Amplifier Supply Voltage (VDDP1-2 pins)	9	24	26.4	V
V_{OFF}	V_{DD} Power Off Voltage	–0.3	0	+0.5	V
T_A	Operating Ambient Temperature	0		+85	°C

1. Unless otherwise specified, all voltages are relative to ground.

4.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground. These parameters are characterized and not fully tested.

Symbol	Parameter[1]	Conditions	Min	Max	Unit
V_{DD}	3.3V Supply Voltage		–0.5	3.6	V
V_{DDP}	Power Amplifier Supply Voltage (VDDP1-2 pins)		–0.3	30	V
V_{OUTMN}	Output Pins vs. Supply Pins (VDDP pins)		–30		V
V_{OUTMX}	Output Pins vs. Ground Pins (VSSP pins)			30	V
I_{MAX1}	Maximum RMS current via power amplifier pins VSSP1, VSSP2	For each pin.		1.5	A
I_{MAX2}	Maximum RMS current via power amplifier pin pairs: VDDP1, VDDP2, OUT1A, OUT1B, OUT2A, OUT2B	A pin pair is connected on board together to the signal trace.		2.3	A
V_I	Input Voltage	5V buffer types	–0.5	5.5	V
		All other buffer types	–0.5	V_{DD} + 0.5	V
		V_{DD} < 0.5V, all digital signals	–0.5	3.47	V
V_O	Output Voltage	All digital signals buffer types	–0.5	V_{DD} + 0.5	V
I_{SINK}	Total NPCP215F Sink or Source Current on digital signals	Total of all output pins		50	mA
	ESD Tolerance	C_{ZAP} = 100 pF, R_{ZAP} = 1.5 KΩ[2]	2000		V
T_{STG}	Storage Temperature		–40	+130	°C
T_{BIAS}	Ambient Temperature Under Bias		0	+85	°C
T_J	Power Amplifier Junction Temperature			130	°C

1. All voltages are relative to ground.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.

4.1.3 Capacitance

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Unit
C_{IO}	I/O Pin Capacitance (digital)	All pins		8	10	pF

1. Not fully tested; characterized only.
2. T_A = 25°C; f = 1 MHz.

4.0 Device Specifications (Continued)

4.1.4 Power Supply Current Consumption under Recommended Operating Conditions

Symbol	Parameter	Power Mode	Conditions[1]	Typ[2]	Max[2]	Unit
I_{DD}	V_{DD} Average[3] Supply Current and Quiet[4] Supply Current	Active	V_{IL} = 0.5V, V_{IH} = 2.4V, DSP clock is 125 MHz	45[5]		mA
I_{DD}	V_{DD} Halt[6] Supply Current	Idle	PLL clock is 125 MHz	15		mA
I_{DD}	V_{DD} Stop[7] Supply Current	Stop		1	1.5[5]	mA
I_{DDPQ}	V_{DDP} Quiet Supply Current	Active	50% PWM output, LC filter and load connected, VDDP = 24V	50		mA
I_{DDPS}	V_{DDP} Standby Supply Current	Standby	Power amplifier in Standby mode, VDDP = 24V	3.5	5	mA

1. Unless stated otherwise, all parameters are specified for 0°C ≤ T_A ≤ 85°C, V_{33} = 3.13V - 3.47V and no resistive load on outputs.
2. Not fully tested; characterized only.
3. Average current is used for power calculation.
4. “Quiet” is defined as “no audio input”.
5. Resistive loads (such as I2C) on outputs may increase this current, especially if LEDs are driven directly from the device.
6. Halt is defined as: DSP clock is halted, PLL and system clocks are on (WAIT instruction execution).
7. Stop is defined as: DSP and system clock is halted, PLL is in power down (Reference clock selected as clock, PLL powered down), Crystal Oscillator is stopped.

4.0 Device Specifications (Continued)

4.2 DC CHARACTERISTICS OF PINS BY I/O BUFFER TYPES

The tables in this section summarize the DC characteristics of all device pins described in Section 1.3 on page 9. The characteristics describe the general I/O buffer types defined in Section 1.2 on page 9. For exceptions, see Section 4.2.5 on page 23.

4.2.1 Input, TTL Compatible

Symbol: T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
I_{ILK}[1]	Input Leakage Current	V_{DD} = 3.13V – 3.47V and 0 < V_{IN} < V_{DD}		±2	µA
I_{ILK5}	5V Input Leakage Current	V_{DD} = 3.13V - 3.47V and V_{DD} < V_{IN} < 5.5V		10	µA

1. For additional conditions, see Section 4.2.5 on page 23.

4.2.2 Input, TTL Compatible, with Schmitt Trigger

Symbol: ST

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.00	5.5	V
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_H	Input Hysteresis		300		mV
I_{ILK}[1]	Input Leakage Current	V_{DD} = 3.13V – 3.47V and 0 < V_{IN} < V_{DD}		±2	µA
I_{ILK5}	5V Input Leakage Current	V_{DD} = 3.13V - 3.47V and V_{DD} < V_{IN} < 5.5V		10	µA

1. For additional conditions, see Section 4.2.5 on page 23.

4.2.3 Output, TTL/CMOS-Compatible, Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL/CMOS-compatible, rail-to-rail push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –*p* mA	2.4		V
		I_{OH} = –50 µA	V_{DD} – 0.2		V
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V
I_{OLK}[1]	Output Leakage Current	V_{DD} = 3.13V – 3.47V and 0 < V_{IN} < V_{DD}		±2	µA

1. For additional conditions, see Section 4.2.5 on page 23.

4.0 Device Specifications (Continued)

4.2.4 Output, TTL/CMOS-Compatible, Open-Drain Buffer

Symbol: OD_n

Output, TTL/CMOS-compatible open-drain output buffer capable of sinking *n* mA. Output from these signals is open-drain and is never forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V
I_{OLK}[1]	Output Leakage Current	V_{DD} = 3.13V – 3.47V and 0 < V_{IN} < V_{DD}		±2	µA

1. For additional conditions, see Section 4.2.5 on page 23.

4.2.5 Notes and Exceptions

1. I_{ILK} and I_{OLK} are measured in the following cases (where applicable):
   - Internal pull-up or pull-down resistor is disabled
   - Push-pull output buffer is disabled (TRI-STATE mode)
   - Open-drain output buffer is at high level
2. Pins that are marked with '5V' in Buffer Type column in sections Section 1.3 on page 9 are 5V tolerant.
   The analog type pins, are not 5V tolerant. This applies if these buffer types are stand-alone or if they are multiplexed with 5V tolerant buffer types.
3. Maximum leakage of all the NPCP215F digital pins together is <30 µA when input voltage is within the supply rails voltage and when PU resistors are disabled in Hi-Z (not fully tested; characterized only).
4. A pin (nRESET) that has an internal static pull-up resistor therefore has leakage current from V_{DD} (when V_{IN} = 0).
5. Strap pins have an internal pull-up resistor enabled during Power-Up reset and therefore may have leakage current from V_{DD} (when V_{IN} = 0).
6. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
7. All digital pins of output type $O_{p/n}$ have a back-drive protection capability of up to 3.6V.

4.2.6 Terminology

Back-Drive Protection. Back-drive protected pins sustain any voltage within the specified voltage limits when the device power supply is off.

5-Volt Tolerance. 5V tolerant pins sustain 5V even if the applied voltage is above the device power supply voltage. A pin is 5V tolerant in the following conditions (where applicable):

- Internal pull-down resistor is disabled. If it is enabled, leakage current is high.
- Push-pull output buffer is disabled (TRI-STATE mode)

Note: If a pin has multiple buffers, the lowest "maximum voltage" among all the buffers is the "maximum voltage" allowed to be applied to the pin.

4.0 Device Specifications (Continued)

4.3 INTERNAL RESISTORS

DC Test Conditions

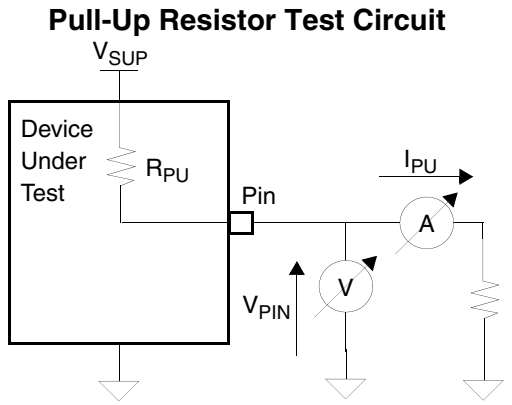


Figure 8. Internal Resistor Test Conditions, T_A = 0°C to 85°C

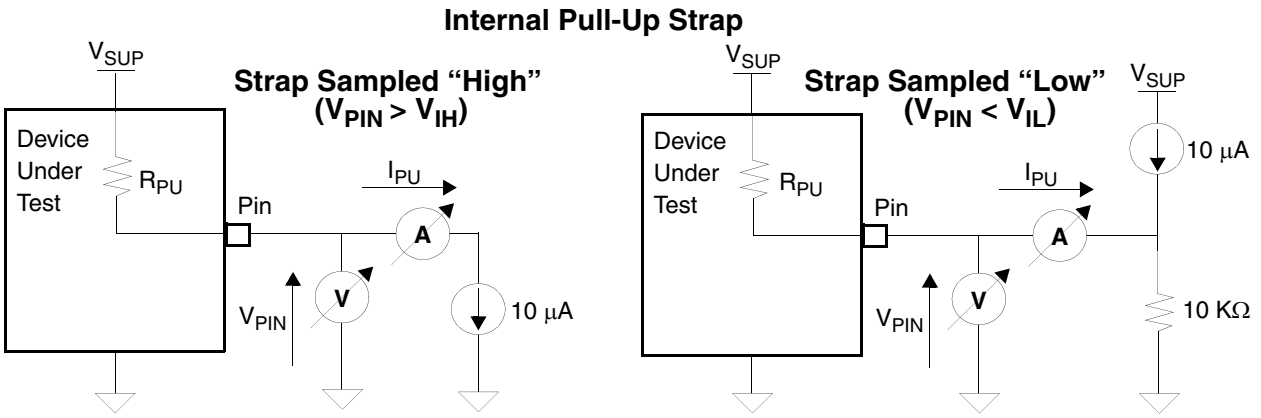


Figure 9. Internal Resistor Design Requirements, T_A = 0°C to 85°C

Notes:
1. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
2. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.

4.3.1 Pull-Up Resistors

Symbol: PU

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-Up Equivalent Resistance for other pins	V_{PIN} = 0V	34	60	95	KΩ

1. TA = 0°C to 85°C, V_{SUP} = 3.3V ±5%.
2. Not fully tested; characterized only.

4.0 Device Specifications (Continued)

4.4 ANALOG CHARACTERISTICS

4.4.1 Power Amplifier Characteristics

Parameter	Symbol	Conditions[1]	Min	Typ	Max	Unit
VDDP to OUT on resistance	R_{ONH}	VDDP = 9V and I_{OUT} of 0.4A		0.2	0.25[2]	Ω
VSSP to OUT on resistance	R_{ONL}	VDDP = 9V and I_{OUT} of 0.4A		0.2	0.25[2]	Ω
Under Voltage Protection limit	V_{UVP}		7.5	8	8.5	V
Over Current Protection Limit	I_{OCP}		5		8	A
OUT Rising Time	T_{RISE}	VDDP = 24V, R_L= 8.2Ω in series to C_L = 1.2nF, 5% to 95%		10		ns
OUT Falling Time	T_{FALL}			10		ns
Continuous Output Power	P_{OB}	Bridge Configuration, VDDP = 24V, F = 1 KHz, THD+N < 1%, R_L= 8Ω V_{Op-p} = 35.8V		20[3]		W
Continuous Output Power	P_{OB}	Bridge Configuration, VDDP = 24V, F = 1 KHz, THD+N < 1%, R_L= 6Ω V_{Op-p} = 31V		20[3]		W
Total Harmonic Distortion + Noise	THD+N	Bridge Configuration, VDDP = 24V, F = 1 KHz, P_O = 15W, R_L= 6Ω			0.5	%
Total Harmonic Distortion + Noise	THD+N	Bridge Configuration, VDDP = 24V, F = 1 KHz, P_O = 1W, R_L= 6Ω			0.25	%
Signal to Noise Ratio	SNR	Bridge Configuration, VDDP = 24V, F = 1 KHz, P_O = 20W, R_L= 6Ω A-Weighed		100		dB
Power Efficiency	η	Bridge Configuration, VDDP = 24V, P_O = 20W, R_L= 6Ω	90			%
Crosstalk		Bridge Configuration, 1 KHz, VDDP = 24V, P_O = 20W, R_L= 6Ω		-80		dB

1. All parameters specified for R_L = Ω, unless otherwise specified.
2. Characterized only.
3. Limited by package Thermal Characteristics; see Section 4.6 on page 35.

4.0 Device Specifications (Continued)

Power Amplifier Typical Performance Graphs

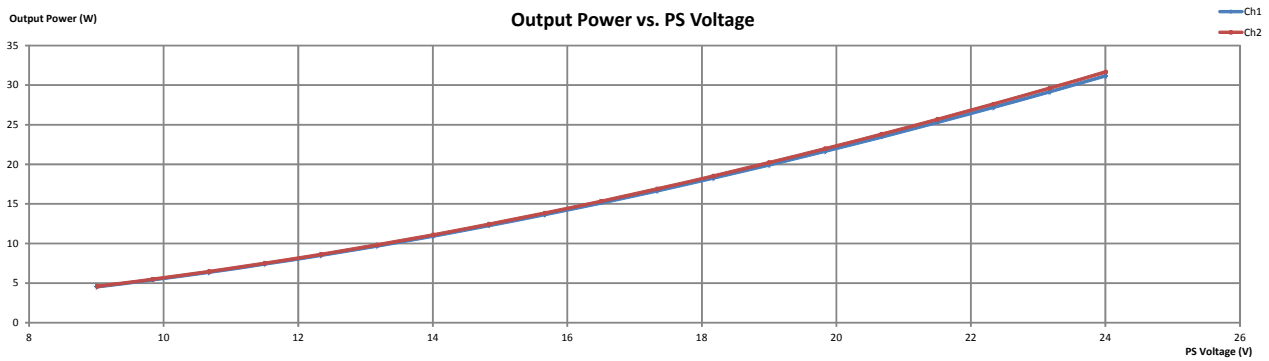
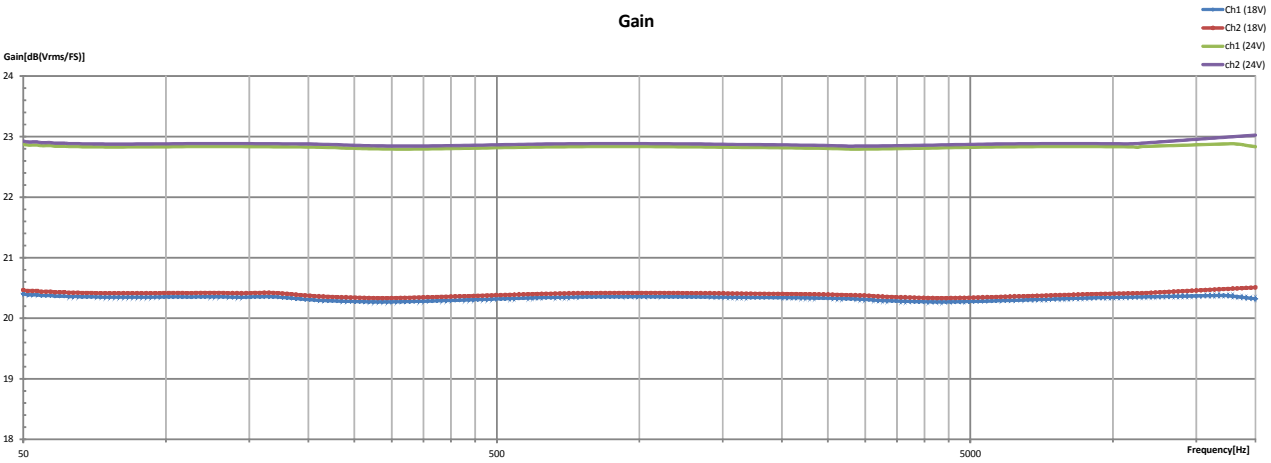


Figure 10. Maximum Output Power vs. Power Supply Voltage (1 KHz, BTL, 6Ω Load)



Note: The measurement is performed without an equalizer.

Figure 11. Gain vs. Frequency (18V and 24V Supply, BTL, 6Ω Load)

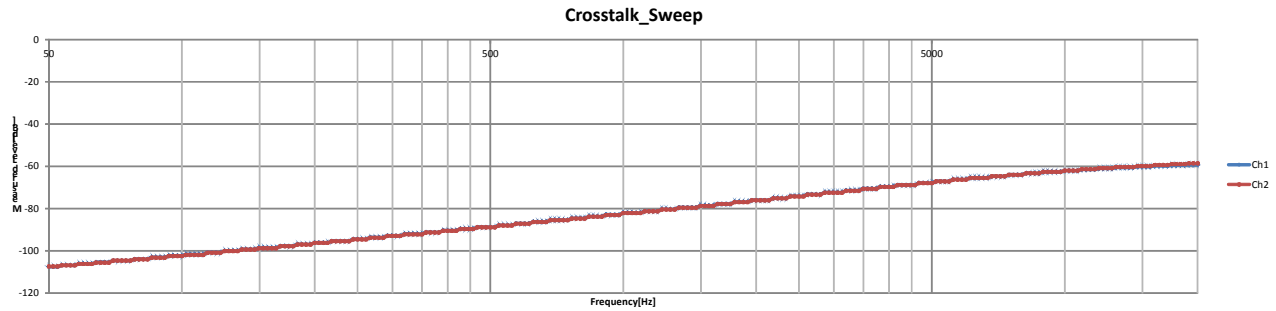


Figure 12. Cross-Talk vs. Frequency (18V to 24V Supply, BTL, 6Ω Load)

4.0 Device Specifications (Continued)

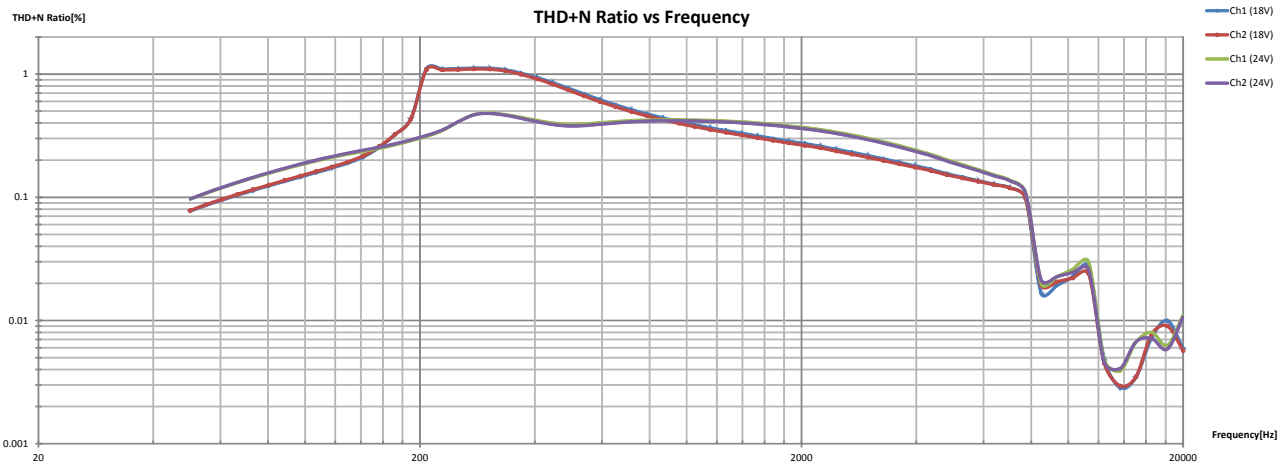


Figure 13. THD+N vs. Frequency (18V and 24V Supply, BTL, 6Ω Load, 15W Output)

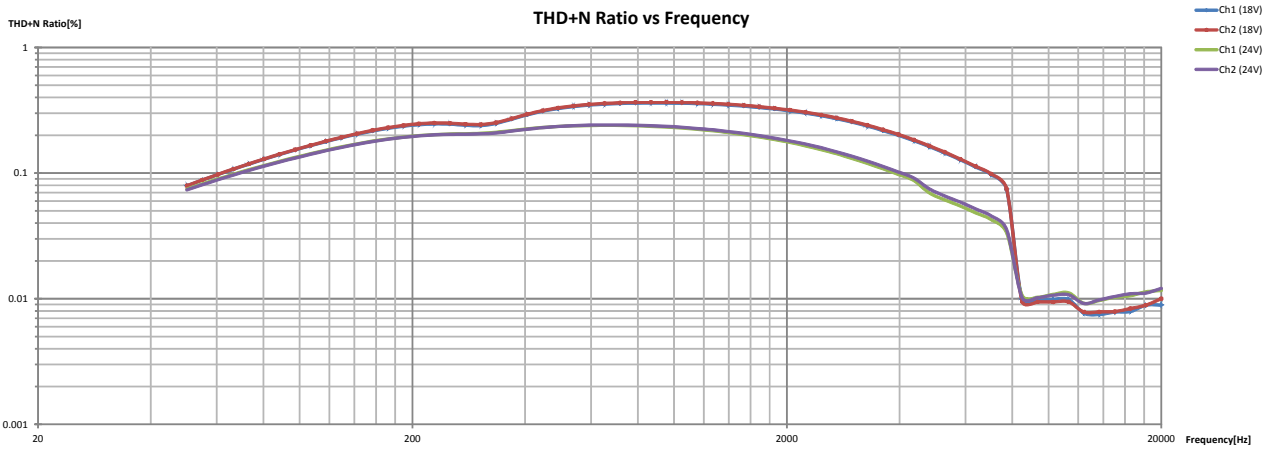


Figure 14. THD+N vs. Frequency (18V and 24V Supply, BTL, 6Ω Load, 1W Output)

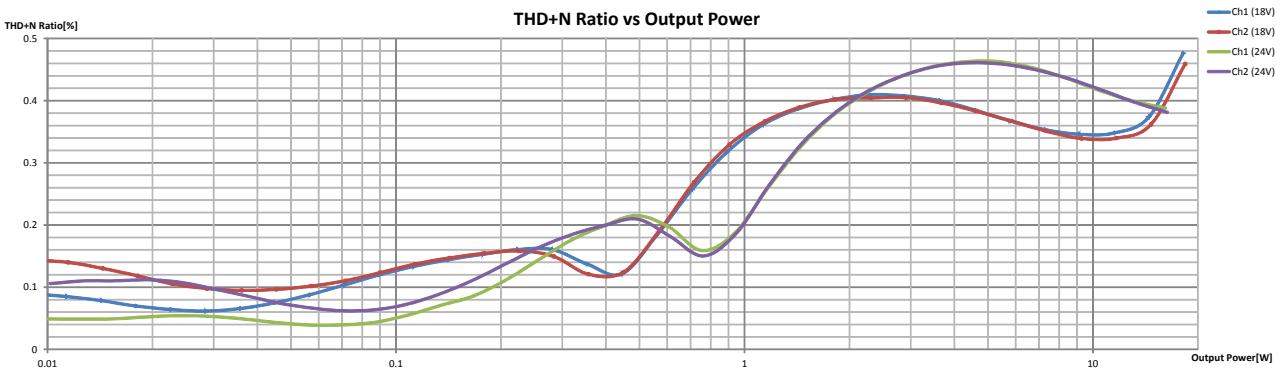


Figure 15. THD+N vs. Output Power (18V and 24V Supply, BTL, 6Ω Load, 1 KHz)

4.0 Device Specifications (Continued)

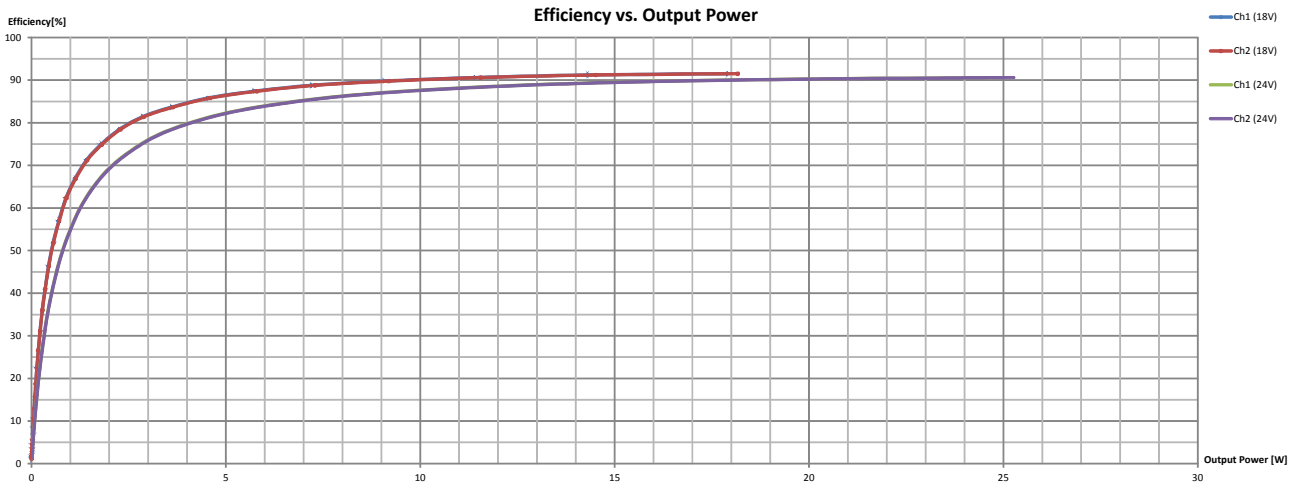


Figure 16. Efficiency vs. Output Power (18V and 24V Supply, BTL, 6Ω Load, 1 KHz)

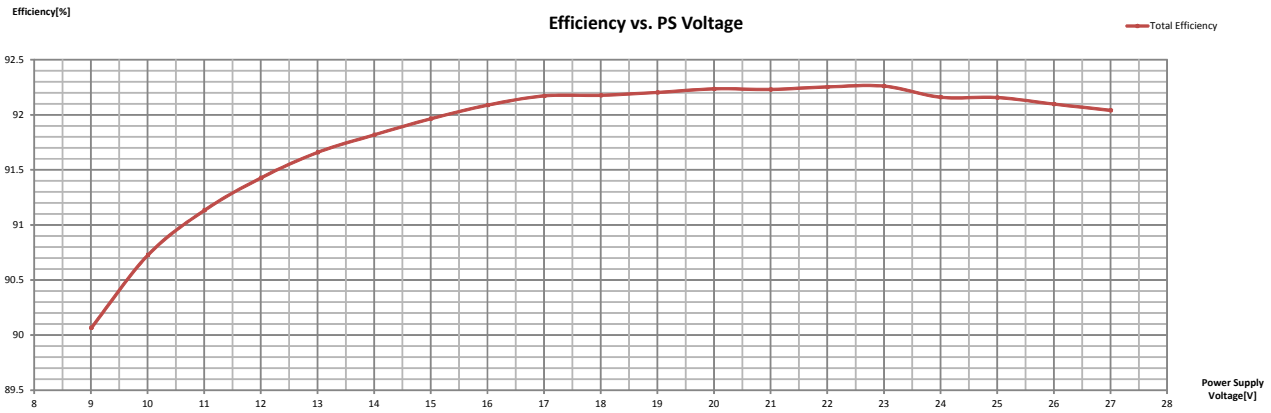


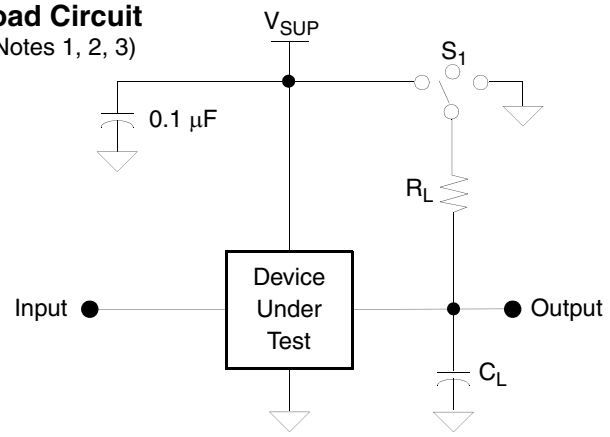
Figure 17. Efficiency vs. Power Supply Voltage (BTL, 8Ω Load, 1 KHz, -3dBFS)

4.0 Device Specifications (Continued)

4.5 AC ELECTRICAL CHARACTERISTICS

4.5.1 AC Test Conditions

Load Circuit
(Notes 1, 2, 3)



AC Testing Input, Output Waveform

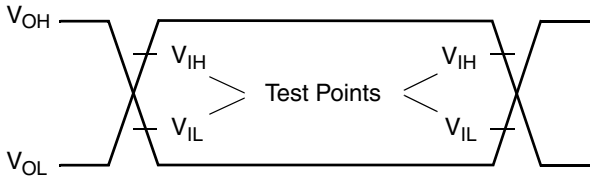


Figure 18. AC Test Conditions, T_A = 0°C to 85°C, V_{SUP} = 3.13V - 3.47V

Notes:

1. V_{SUP} is V_{33} according to the power well of the pin, relevant for all signals at LVTTL levels.
2. C_L = 50 pF for all output pins except the following pin groups (values include both jig and oscilloscope capacitance)
   C_L = 100 pF for I2C
   C_L = as otherwise defined
3. S_1 = Open – for push-pull output pins
   S_1 = V_{SUP} – for high-impedance to active-low and active-low to high-impedance transition measurements
   S_1 = GND – for high-impedance to active-high and active-high to high-impedance transition measurements
   R_L = 1.0 KΩ – for all pins
4. The following abbreviations are used in Section 4.5: RE = Rising Edge; FE = Falling Edge.

Definitions

The timing specifications in this section are relative to V_{IL} or V_{IH} (according to the specific buffer type) on the rising or falling edges of all the signals, as shown in the following figures (unless specifically stated otherwise).

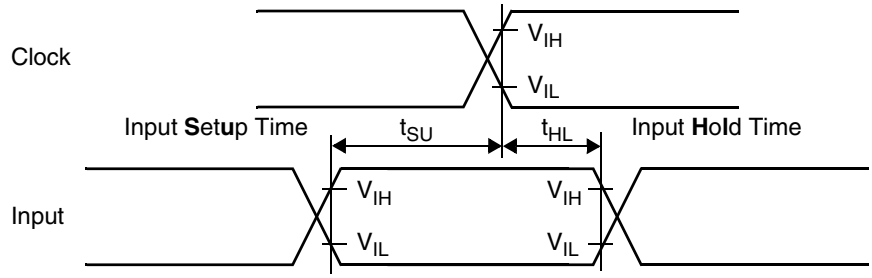


Figure 19. Input Setup and Hold Time

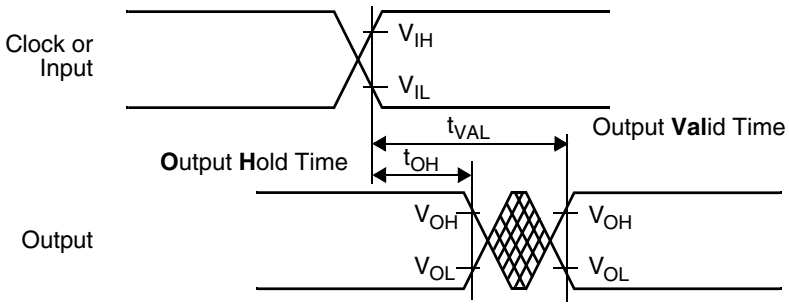


Figure 20. Clock-to-Output and Propagation Delay

4.0 Device Specifications (Continued)

4.5.2 Reset Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
t_{CORD}	21	Power-Up Requirement: all power supplies at valid level until nRESET deasserted[1]	After reset delay	5		ms
t_{PUS}	21	V_{DD} valid before V_{DDP} rising	Power-up sequence	0	20	ms
t_{PRST}	21	nRESET Pulse Width	To assure reset	1		ms
t_{RSTC}	21	Internal reset delay after nRESET deasserted	REF latched high	11000	12500	t_{REFCLK}
			REF latched low	48000	52000	t_{REFCLK}
$t_{CLKRSTD}$	21	Stable reference clock to reset end		100		µs
t_{STSU}	21	Valid straps signals level setup time to nRESET rising		100		µs
t_{STH}	21	Valid straps signals level hold after nRESET rising		10		t_{REFCLK}
t_{OE}	21	Internal reset end to outputs enabled on strap pins		-100		t_{REFCLK}

1. Requirement for system.

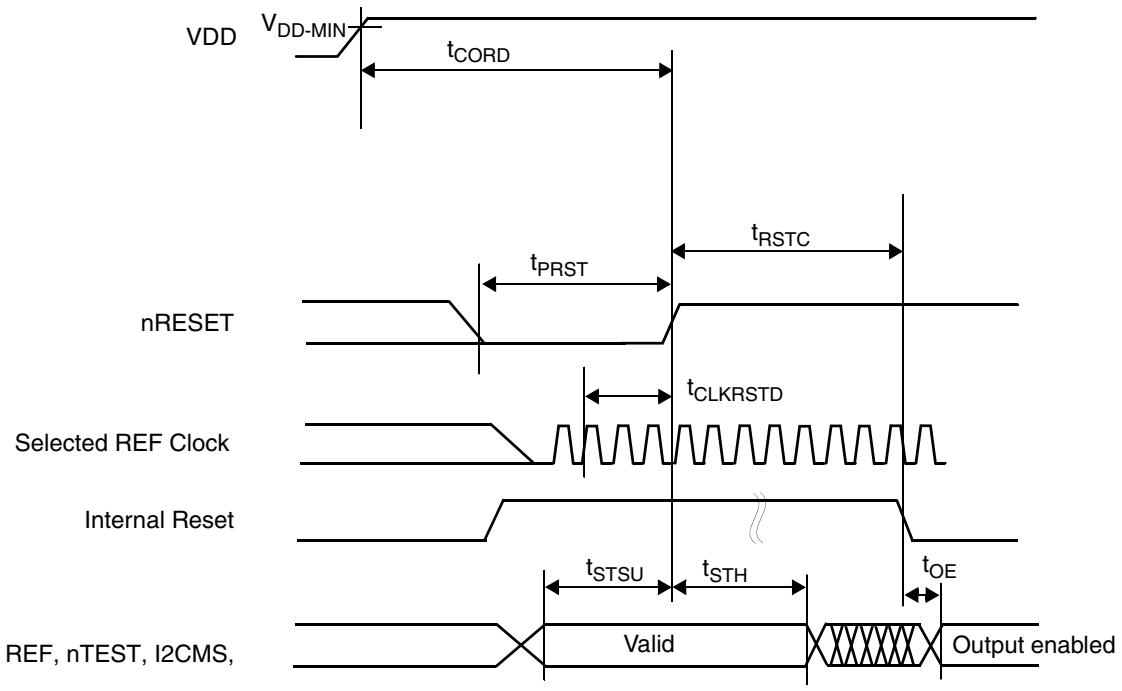


Figure 21. Device Reset

4.0 Device Specifications (Continued)

4.5.3 Clock Timing

CLKREF (DCLK or Oscillator) Clock Timing

Symbol	Figure	Description	Conditions	Min	Typ	Max	Units
t_{REFCLK}	22	CLKREF Average Clock Period	From RE to RE of CLKREF	40		1000	ns
A_{CLK}		CLKREF Accuracy	For a specific system		50	100	ppm
t_{CLKH}	22	CLKREF High Time	From RE to FE of CLKREF	35			ns
t_{CLKL}	22	CLKREF Low Time	From FE to RE of CLKREF	35			ns
t_{CLKR}	22	CLKREF Rise Time	From 0.8V to 2.0V			5	ns
t_{CLKF}	22	CLKREF Fall Time	From 2.0V to 0.8V			5	ns
Duty Cycle		CLKREF Duty Cycle	At 1.4V	40		60	%
J_{PERIOD}		Period Jitter[1]	At 1.4V			1.5	ns
J_{CTC}		Cycle-to-Cycle RMS Jitter	At 1.4V			250	ps

1. Measured over a 20 μs window.

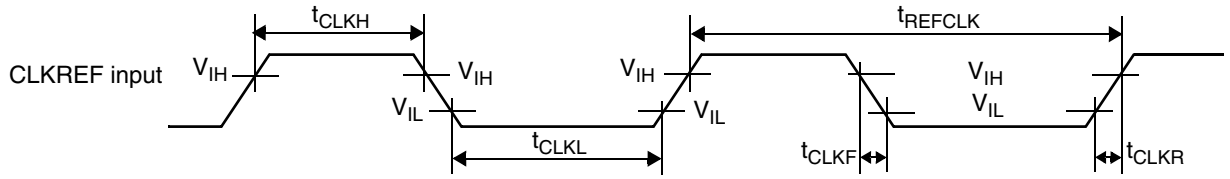


Figure 22. CLKREF Clock Waveforms

CLKOUT Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
t_{CLK}	23	CLKOUT Clock Period	From RE to RE of CLKOUT, C_L = 20 pF	50		ns
t_{CLKH}	23	CLKOUT High Time[1]	From RE to FE of CLKOUT, C_L = 20 pF	15		ns
t_{CLKL}	23	CLKOUT Low Time[1]	From FE to RE of CLKOUT, C_L = 20 pF	15		ns
t_{CLKR}	23	CLKOUT Rise Time[1]	From V_{IL} to V_{IH} of CLKOUT, C_L = 20 pF		5	ns
t_{CLKF}	23	CLKOUT Fall Time[1]	From V_{IH} to V_{IL} of CLKOUT, C_L = 20 pF		7.5	ns
D_{CLK}		CLKOUT Duty Cycle[1]	C_L = 20 pF	28		%

1. Not fully tested; characterized only.

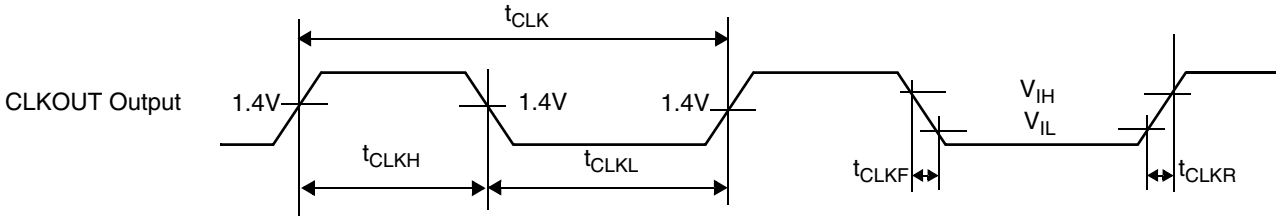


Figure 23. CLKOUT Clock Waveforms

4.0 Device Specifications (Continued)

4.5.4 Input Signal Detection Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
t_{SSCL}	24	Debounced SCL input pulse width (which guarantees detection)		15		ns

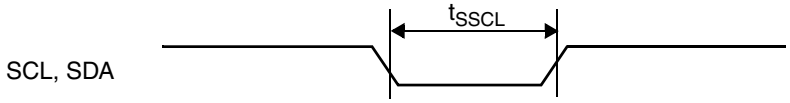


Figure 24. Input Signal Detection Timing

4.5.5 I2C Slave Timing

Symbol	Figure	Description	Conditions	Min	Max	Units
f_{SCL}	25	SCL Frequency	At 1.3V SCL RE to RE		400[1]	KHz
t_{LOW}		SCL Low Time	At 0.8V (both edges)	0.5		µs
t_{HIGH}	25	SCL High Time	At 2.0V (both edges)	0.26		µs
t_{I2CR}	25	SCL, SDA Rise Time	From 0.8V to 2.0V[1]		0.25[2]	µs
t_{I2CF}	25	SCL, SDA Fall Time	From 2.0V to 0.8V[1]		100	ns
$t_{SU:DAT}$	25	SDA Setup Time	Before SCL RE	50		ns
$t_{HD:DAT}$	26	SDA Hold Time	After SCL FE	**0**		ns
$t_{SU:STA}$	26	SCL Setup Time	Before Restart condition	0.26		µs
$t_{HD:STA}$	26	SCL Hold Time	After Start/Restart condition	0.26		µs
$t_{SU:STO}$	26	SCL Setup Time	Before Stop condition	0.26		µs
t_{BUF}	26	Bus Free Time	Between Stop and Start conditions	0.5		µs
$t_{VD:DAT}$	26	Data Valid Time	After SCL FE		0.45	µs
$t_{VD:ACK}$	26	Data Valid Acknowledge Time	After SCL FE		0.45	µs

1. Test conditions: R_L = 1 KΩ to V_{DD} = 3.3V, C_L = 100 pF to GND.
2. Not tested; based on design simulation.

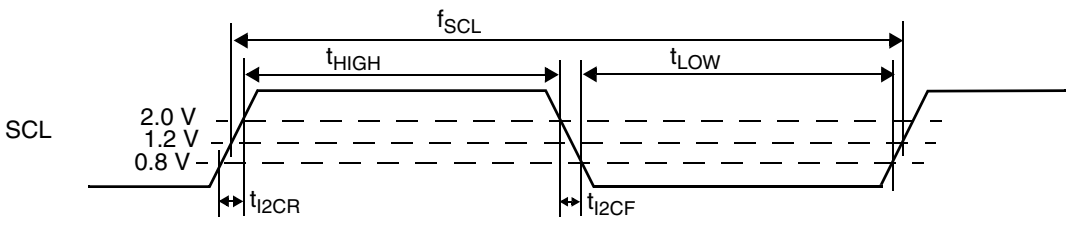


Figure 25. I2C SCL Signal Timing

4.0 Device Specifications (Continued)

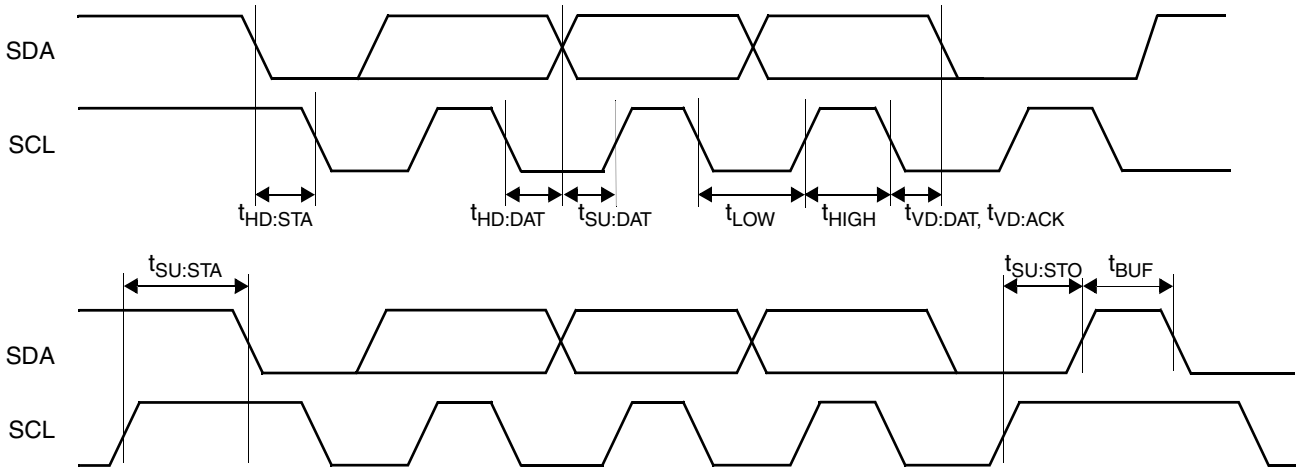


Figure 26. I2C Timing

4.5.6 I2C Master Timing

Symbol	Figure	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	25	SCL Frequency[5]	Programming capability	f_{AEE}[1]/ 16384		f_{AEE} / 8	
		SCL Frequency[5]	At 1.3V SCL RE to RE	0		400 [2]	KHz
t_{LOW}	25	SCL Low Time[5]	At 0.8V (both edges)	8 x T_{AEE}[3]	0.5 x T_{SCL}[4]		
t_{HIGH}	25	SCL High Time[5]	At 2.0V (both edges)	8 x T_{AEE}	0.5 x T_{SCL}		
t_{I2CR}	25	SCL, SDA Rise Time	From 0.8V to 2.0V[2]			0.25[5]	µs
t_{I2CF}	25	SCL, SDA Fall Time[5]	From 2.0V to 0.8V[2]			100	ns
$t_{SU:DAT}$	26	SDA Setup Time[5]	Before SCL RE	4 x T_{AEE}	0.25 x T_{SCL}		
$t_{HD:DAT}$	26	SDA Hold Time[5]	After SCL FE	4 x T_{AEE}	0.25 x T_{SCL}		
$t_{SU:STA}$	26	SCL Setup Time[5]	Before Restart condition	12 x T_{AEE}	0.5 x T_{SCL}		
$t_{HD:STA}$	26	SCL Hold Time[5]	After Start/Restart condition	4 x T_{AEE}	0.5 x T_{SCL}		
$t_{SU:STO}$	26	SCL Setup Time[5]	Before Stop condition	4 x T_{AEE}	0.5 x T_{SCL}		
t_{BUF}	26	Bus Free Time[5]	Between Stop and Start conditions	16 x T_{AEE}	0.5 x T_{SCL}		
$t_{VD:DAT}$	26	Data Valid Time[5]	After SCL FE	4 x T_{AEE}	0.5 x T_{SCL}		
$t_{VD:ACK}$		Data Valid Acknowledge Time[5]	After SCL FE	4 x T_{AEE}	0.5 x T_{SCL}		

1. f_{AEE} is the Audio Enhancing Engine system clock frequency.
2. Test conditions: R_L = 1 KΩ to V_{DD} = 3.3V, C_L = 100 pF to GND.
3. T_{AEE} is the Audio Enhancing Engine system clock period.
4. T_{SCL} is the SCL clock period ($1/f_{SCL}$).
5. Not tested; based on design simulation.

4.0 Device Specifications (Continued)

4.5.7 SSI Timing

Symbol	Figure	Description	Conditions	Min	Typ	Max	Units
t_T	27	DCLK Cycle Time	At 1.3V DCLK RE to RE	1/64	1/64	1/32	$1/F_S$[1]
f_{DCLK}		DCLK Frequency		32	64	64	F_S[1]
t_{LOW}	27	DCLK Low Time	At 0.8V (both edges)	0.35	0.5		t_T
t_{HIGH}	27	DCLK High Time	At 2.0V (both edges)	0.35	0.5		t_T
t_{HTR}	27	Output Hold Time	After DCLK RE	15 ns	0.5 * t_T		
t_{DTR}	27	Output Valid Time	After DCLK RE		0.5	0.75	t_T
t_{HR}	27	Input Hold Time	After DCLK RE	3			ns
t_{SR}	27	Input Setup Time	Before DCLK RE	0.2			t_T

1. F_S is the audio sampling frequency.

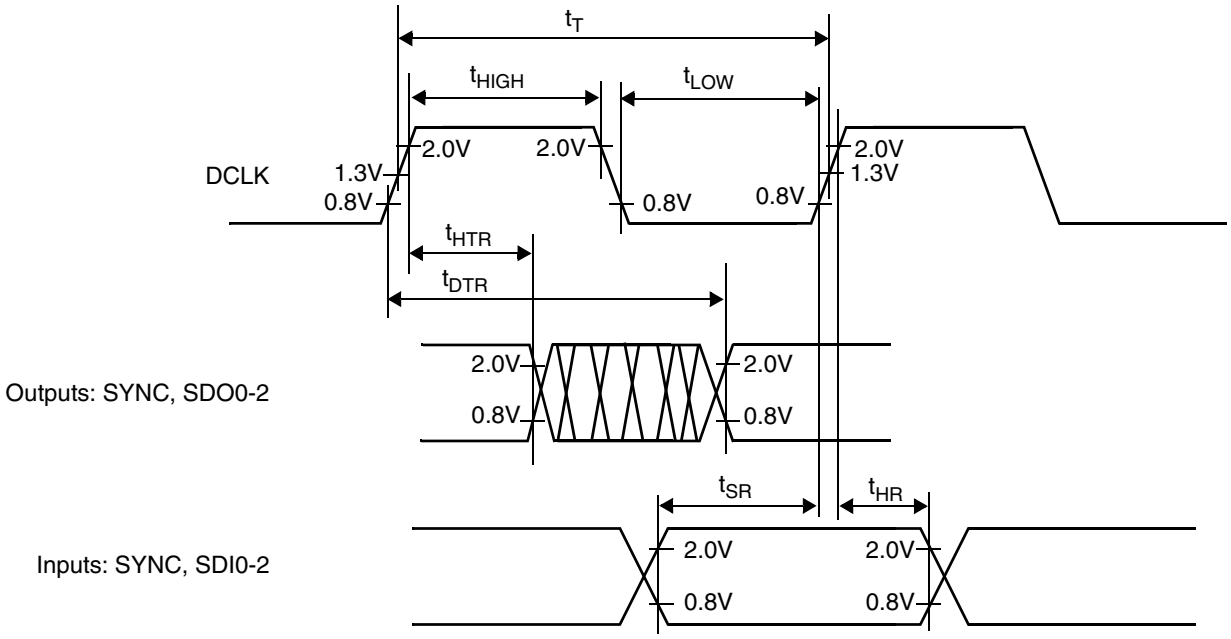


Figure 27. SSI Signal Timing

4.0 Device Specifications (Continued)

4.6 PACKAGE THERMAL INFORMATION

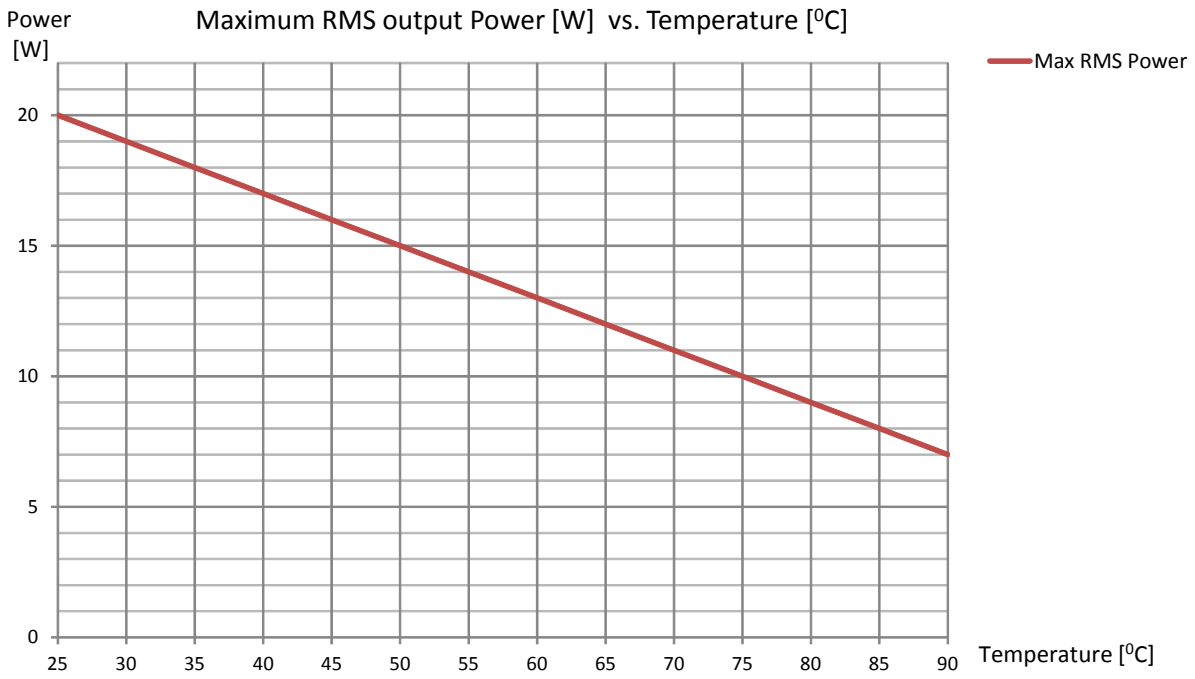
Thermal resistance (degrees ^{O}C/W) Theta$_{JA}$ values for the NPCP215F package are as follows:

Table 3. Theta (Θ) J-A Value Targets

	Θ_{JA} (Degrees Kelvin/Watt) Target		
Package	**0 m/s**	**1 m/s**	**2 m/s**
48-Pin QFN	22	19	18

Note: All values apply to a device soldered to a 4-layer PCB, with the metal plate on the bottom of the device fully soldered to a metal surface on the PCB, with 72 vias to PCB ground plane and to a metal surface on the solder side.

RMS Output Power Derating



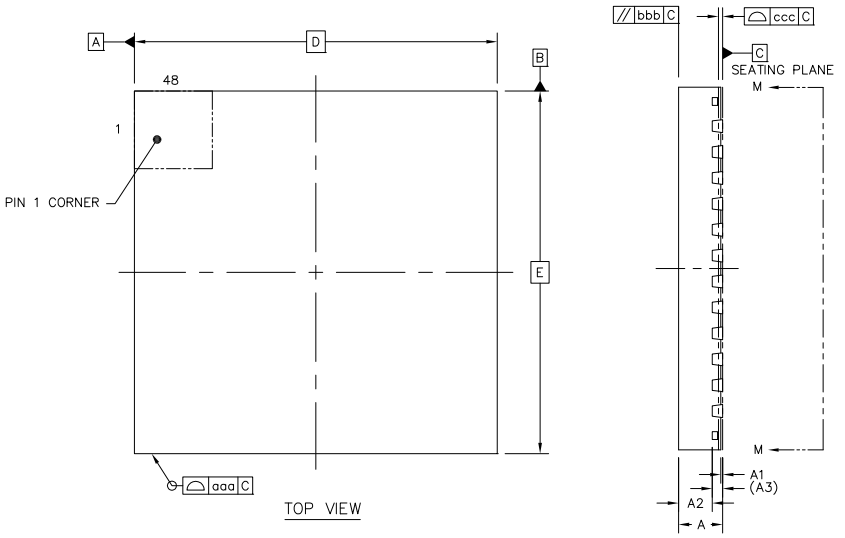
Conditions: V_{DDP} = 24 V, still air, 4 layers PCB with an area of 5000 mm^2 and 1 oz copper thickness. Both channels active, 1 KHz Sine wave.

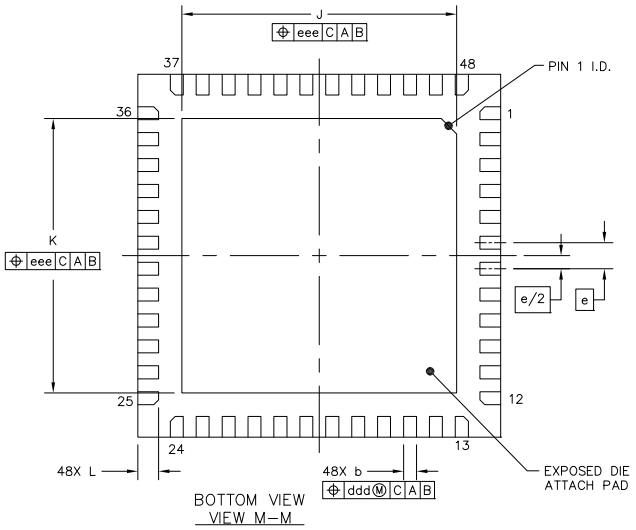
Note: The total output power from the device is 2x the numbers in the diagram.

Figure 28. Maximum Output Power vs. Ambient Temperature (1 KHz, BTL, 6Ω Load)

QFN48 Physical Dimensions

Control dimensions are in millimeters.





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

48-Pin Quad Flat No-Lead (QFN) Package
Order Number: NPCP215FA0YX

Device topside mark specification:

1st Line: **Nuvoton Company Logo.**
2nd Line: **Part number - NPCP215xA0YX ('x' is B or F)**
('Y': QFN package number; 'X': Green package finish indicator.)
3rd Line: **Assembly Lot Number - XXXXXXXX–XXX.**
4th Line: **Tracking code - YWWXXXX, where YWW is the Date Code and XXXX is Nuvoton proprietary information.**

Date code: **YWW, where Y is the year and WW is the week. For example, date code 235 indicates that device assembly was done on week 35, year 2012.**

nuvoTon

NPCP215FA0YX

XXXXXXXX–XXX

YWWXXXX

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