ARM® Cortex®-M4F

32-bit Microcontroller

NPCA121 Series
Audio Enhancing Engine
Preliminary Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NPCA121 series is a member of Nuvoton sound enhancing family based on 32-bit ARM® Cortex®-M4F core with DSP extensions and a Floating Point Unit which runs up to 200 MHz with 512 KB of flash memory and 192 KB of SRAM. It supports Bongiovi Digital Power Station (DPS) V3D™ virtual sound enhancing algorithms, optimized for consumer products like gaming headset and audio headphone.

The NPCA121 supports plenty of audio peripherals such as I2S, DMIC and audio DPWM modulator. It also equipped with a variety of peripherals, such as Multi-Function Timers, Watchdog Timers, RTC, PDMA, UART, SPI, I^2C, PWM, GPIO, 12-bit ADC, USB1.1 Device, Low voltage reset and Brown-out Detector.

Bongiovi Digital Power Station (DPS) premium algorithms includes below

- ◯ Bongiovi AGC
- ◯ 10 + 2 bands of parametric EQ
- ◯ Mono, 1.1, 2.0 and 2.1 Speakers Stereo Configuration Only
- ◯ Look-ahead limiter
- ◯ Dynamic Stereo Enhancement
- ◯ Noise Gate
- ◯ Virtual Subwoofer bass enhancement
- ◯ V3D™ Headphone Virtual Surround Algorithm

The NPCA121 series is suitable for a wide range of applications such as:

- Audio Enhancing Platform
- Consumer Audio Products
- Gaming Headset
- Audio Headphone

2 FEATURES

2.1 NPCA121 Series Features

- Core
  - ARM® Cortex®-M4F core running up to 200 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Low Power Sleepmode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
  - Supports Embedded Trace Macrocell
- Built-in LDO for wide operating voltage range
- Flash Memory
  - 512 KB on-chip Application ROM (APROM)
  - Configurable program code/data allocation
  - 4 KB on-chip Flash for user-defined loader (LDROM)
  - Supports 2-wire ICP update through SWD/ICE interface
  - Supports In-system program (ISP), In application program (IAP) update
  - Supports 4 KB page erase for all embedded flash
  - Supports 4 KB two-way cache to reduce power consumption and improve performance.
  - Enhanced performance up to 3.4 Core Mark/MHz when running code in Flash with cache
  - Supports 2-wire ICP flash updating through SWD interface
  - Supports 32-bit/64-bit and multi-word flash programming function.
  - Supports fast flash programming verification by CRC function.
- SRAM
  - 192 KB embedded SRAM
  - 32 KB SRAM in bank 0 that supports hardware parity check and retention mode
  - Supports byte-, half-word- and word-access
  - Supports exception (NMI) generated once a parity check error occurs
  - Supports PDMA mode
- Clock Control
  - Built-in 48.0 MHz or 49.152 MHz selectable internal high speed RC oscillator (HIRC) for system operation.
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation.
  - 4~24.576 MHz external high speed crystal oscillator (HXT) for precise timing operation.
  - 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation.
  - Supports one PLL up to 500 MHz for high performance system operation, sourced from HIRC or HXT.
  - Supports clock failure detection for high/low speed external crystal oscillator.
  - Supports exception (NMI) generation once a clock failure detected.
  - Supports clock output.
- GPIO
  - Supports four I/O modes:
    - Quasi bi-direction

- Push-Pull output
- Open-Drain output
- Input only with high impendence

- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high slew driver and high sink current I/O (up to 20mA at 3.3V)
- Supports software selectable slew rate control
- Supports 5V tolerance function on subset of GPIO except analog I/O

- PDMA (Peripheral DMA)
  - Supports 16 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports stride function.
  - Channel 0, 1 supports time-out function for each channel.
  - Supports Basic and Scatter-Gather Transfer modes
  - Each channel supports circular buffer management using Scatter-Gather Transfer mode
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports single and burst transfer type
  - Supports source and destination address can be increment or fixed.
  - DMA transfer count up to 65536.
- Multi-Function Timer (MFT, Timer + PWM)
  - TIMER mode
    - Supports 4 sets of 32-bit timers with 24-bit up-timer and 8-bit prescale counter, 24-bit up counter value is readable.
    - Independent clock source for each timer
    - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
    - Supports event counting function to count the event from external pin
    - Supports input capture function to capture or reset counter value
    - Supports external capture pin event for interval measurement.
    - Supports external capture pin event to reset 24-bit up counter.
    - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
    - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and DMA.
    - Supports Inter-Timer trigger mode
  - PWM mode
    - Supports four 16-bit PWM counters with 10-bit dead time generator
    - Supports 12-bit pre-scale for PWM.
    - Supports independent mode for PWM output channel
    - Supports 8 channel PWM outputs in complementary mode
    - Supports mask function and tri-state enable for each PWM pin
    - Supports interrupt on the following events:
      - PWM counter match zero, period value or compared value
    - Supports trigger EADC on the following events:
      - PWM counter match zero, period value or compared value
- PWM
  - Supports up to 6 independent PWM outputs with 16-bit resolution
  - Supports maximum clock frequency up to 200MHz
  - Supports 12-bit clock prescale
  - Supports dead time with maximum divided 12-bit prescale
  - Supports one-shot or auto-reload counter operation mode
  - Supports up, down or up-down PWM counter type
  - Supports synchronous function for phase control
  - Supports counter synchronous start function

- Supports complementary mode for 3 complementary paired PWM output channel
- Supports brake function with auto recovery after brake condition removed
- Supports mask function and tri-state output for each PWM channel
- Supports trigger EADC to start conversion
- Supports up to 6 independent input capture channels with 16-bit resolution counter

- Watchdog Timer
  - 18-bit free running up counter for WDT time-out interval
  - Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
  - Configurable to force WDT enable after chip power-on or reset.
  - Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
- Window Watchdog Timer
  - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
  - Window set by 6-bit counter with 11-bit prescale
  - WWDT counter suspends in Idle/Power-down mode
- RTC
  - Supports software compensation by setting frequency compensate register (FCR),compensated clock accuracy reaches ±5ppm within 5 seconds
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports Day of the Week counter
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports 1 Hz, clock output
  - Supports wake-up from idle mode, Power-down mode and Standby Power-down mode
  - Supports 32 kHz Oscillator gain control
  - Supports RTC Time Tick and Alarm Match interrupt
  - Support Time stamp
- UART
  - Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped
  - Support baud rate up to 12.5 MHz
  - Supports 16-byte FIFOs with programmable level trigger
  - Supports auto flow control (CTS and RTS)
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Programmable receiver FIFO trigger level
  - Supports wake-up function
  - Supports 8-bit receiver FIFO time-out detection function
  - Supports Auto-Baud Rate measurement and baud rate compensation function
  - Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function
  - Supports nCTS, incoming data, RX FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode.
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction

- Supports PDMA mode

- I²C
  - Supports up to two sets of I²C devices
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Supports 10 bits mode
  - Support High speed mode 3.4Mbps
  - Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports SMBus and PMBus
  - Supports multi-address Power-down wake-up function
- I²S
  - Supports one I²S interface
  - Interface with external audio CODEC
  - Supports Master and Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Mono and stereo audio data
  - I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
  - PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
  - PCM protocol supports TDM multi-channel transmission in one audio sample, the number of data channels can be set as 2, 4, 6, or 8
  - Two 16-level FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- SPI0
  - SPI Quad controller – SPI0
  - Supports Master or Slave mode operation
  - Supports 2-bit Transfer mode
  - Supports Dual and Quad I/O Transfer mode
  - Supports one/two data channel half-duplex transfer
  - Support receive-only mode
  - Configurable bit length of a transfer word from 8 to 32-bit
  - Provides separate 8-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports the byte reorder function
  - Supports Byte or Word Suspend mode
  - Supports 3-wired, no slave select signal, bi-direction interface
  - Master up to 25 MHz, and Slave up to 25 MHz (when chip operating at V_{DD} = 2.7~3.6V)
  - Supports PDMA mode
- SPI / I²S
  - Supports two sets of SPI/ I2S controllers – SPI1/ SPI2
  - Supports Master or Slave mode operation
  - Supports two PDMA requests, one for transmitting and the other for receiving
  - SPI supports configurable bit length of a transfer word from 8 to 32-bit

- SPI Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
- SPI supports MSB first or LSB first transfer sequence
- SPI supports the byte reorder function
- SPI supports Byte or Word Suspend mode
- SPI supports one data channel half-duplex transfer
- SPI supports receive-only mode
- I2S interface with external audio CODEC
- I2S supports Master and Slave mode
- I2S supports 8-, 16-, 24- and 32-bit audio data sizes
- I2S supports mono and stereo audio data
- I2S supports PCM mode A, PCM mode B, I2S and MSB justified data format
- I2S Interface with external audio CODEC
- I2S provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary

- EADC
  - Analog input voltage range: 0~ AV_{DD}
  - Supports single 12-bit SAR EADC conversion
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Up to 13 external single-ended analog input channels
  - Up to 2 MSPS conversion rate
  - Supports three power saving modes:
    - Deep Power-down mode
    - Power-down mode.
    - Standby mode.
  - Supports single EADC interrupt
  - Supports calibration and load calibration words capability.
  - An A/D conversion can be triggered by Software enable, External pin, Timer 0~3 overflow pulse trigger and PWM trigger.
  - 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
  - Maximum EADC clock frequency is 60 MHz.
  - Configurable EADC internal sampling time.
  - Up to 13 sample modules
    - Each of sample module 0~12 which is configurable for EADC converter channel EADC_CH0~12 and trigger source.
    - Double buffer for sample module 0~3
    - Configurable sampling time for each sample module.
    - Conversion results are held in 13 data registers with valid and overrun indicators.
  - Supports PDMA transfer
- USB 1.1 Device Controller
  - Compliant with USB 2.0 Full-Speed specification
  - Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
  - Supports Control/Bulk/Interrupt/Isochronous transfer type
  - Supports suspend function when no bus activity existing for 3 ms
  - Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1k bytes buffer size
  - Provides remote wake-up capabilityProgrammable initial value
- Digital Microphone Inputs
  - Provides one 32-level FIFO data buffers for receiving.
  - Generates interrupt requests when buffer levels cross a programmable boundary.
  - Supports PDMA transfer.

- Supports up to four channel digital microphones.
- Both digital PDM microphone inputs can be used simultaneously.

- Voice Active Detection
  - Configuration detect levels.
  - Supports idle mode wake-up function.
  - Supports auto switch DMIC path when CPU wake-up by VAD.
  - Generates interrupt requests when voice detected.
- Audio DPWM Modulator
  - Differential Audio PWM Output (DPWM)
  - Supports left channel, right channels and sub-woofer channel.
  - Supports sample rate from 16~96 kHz
  - Programmable biquad filter with 10 band.
  - PDMA data channel for streaming of PCM audio data.
  - Supports the single precision floating point for input data and BIQ coefficient.
  - Provides one 32-level FIFO data buffers for transmitting.
- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports 8-/16-/32-bit of data width
  - Programmable seed value
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
  - Supports using DMA to write data to perform CRC operation
- Brown-out Detector
  - With 8 levels: 3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 1.5V
- Operating Temperature: -40℃~85℃
- Packages
  - All Green package (RoHS)
  - QFN 48-pin (6x6 mm)
  - LQFP 64-pin (7x7 mm)

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
DMIC	Digital Microphone Inputs
DPWM	Audio DPWM Modulator
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	High Speed RC Oscillator
HXT	External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
VAD	Voice Active Detection
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Parts Information

PART NUMBER		NPCA1	
		21DD	21DY
Max. CPU frequency (MHz)		200	
Flash (KB)		512	
SRAM (KB)		192	192
ISP Loader ROM (KB)		4	
I/O		57	41
32-bit Timer		4	
RTC		√	
Connectivity	UART	1	
	SPI	1	
	SPI/I²S	2	
	I²S	1	
	I²C	2	
PWM		6	5
USB 1.1 FS Device		√	
12-bit ADC		13	12
Audio Function	Audio DPWM	2.1	-
	VAD	√	-
	DMIC	4	-
Package		LQFP 64 (7x7 mm)	QFN 48 (6x6 mm)
Status		Released	In Developing

Table 4.1-1 Devices Features and Peripheral Counts

4.2 Ordering Information

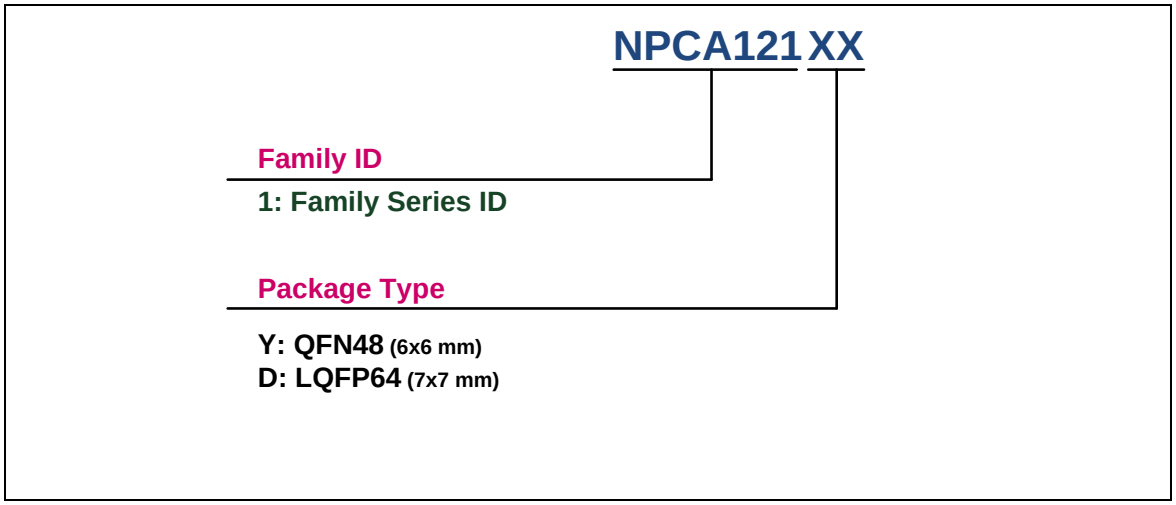


Figure 4.2-1 Ordering Information Scheme

4.3 Pin Configuration

4.3.1 QFN48 (6x6 mm) Pin Diagram

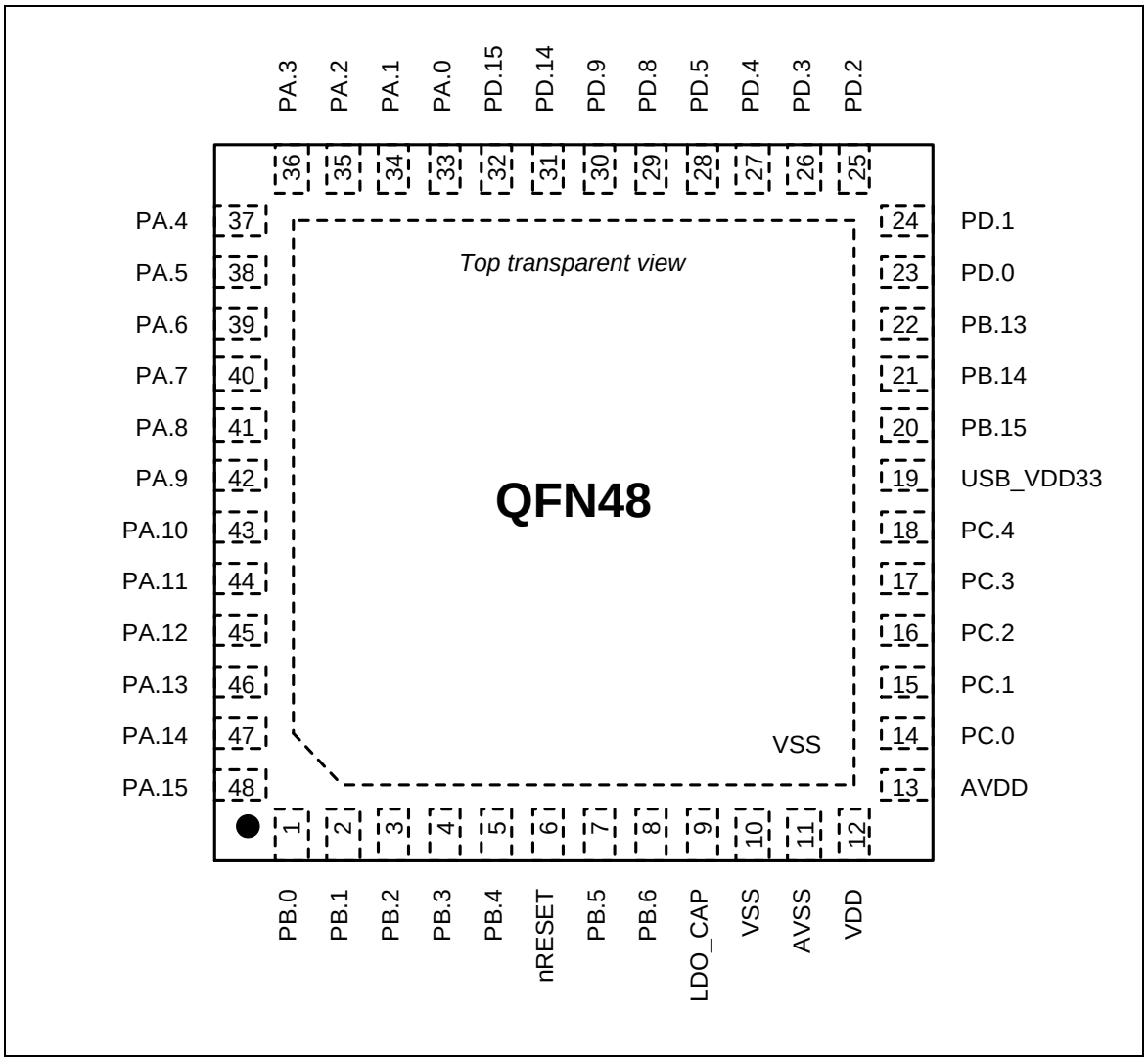


Figure 4.3-1 QFN48 (6x6 mm) Pin Diagram (In Developing)

4.3.2 LQFP64 (7x7 mm) Pin Diagram

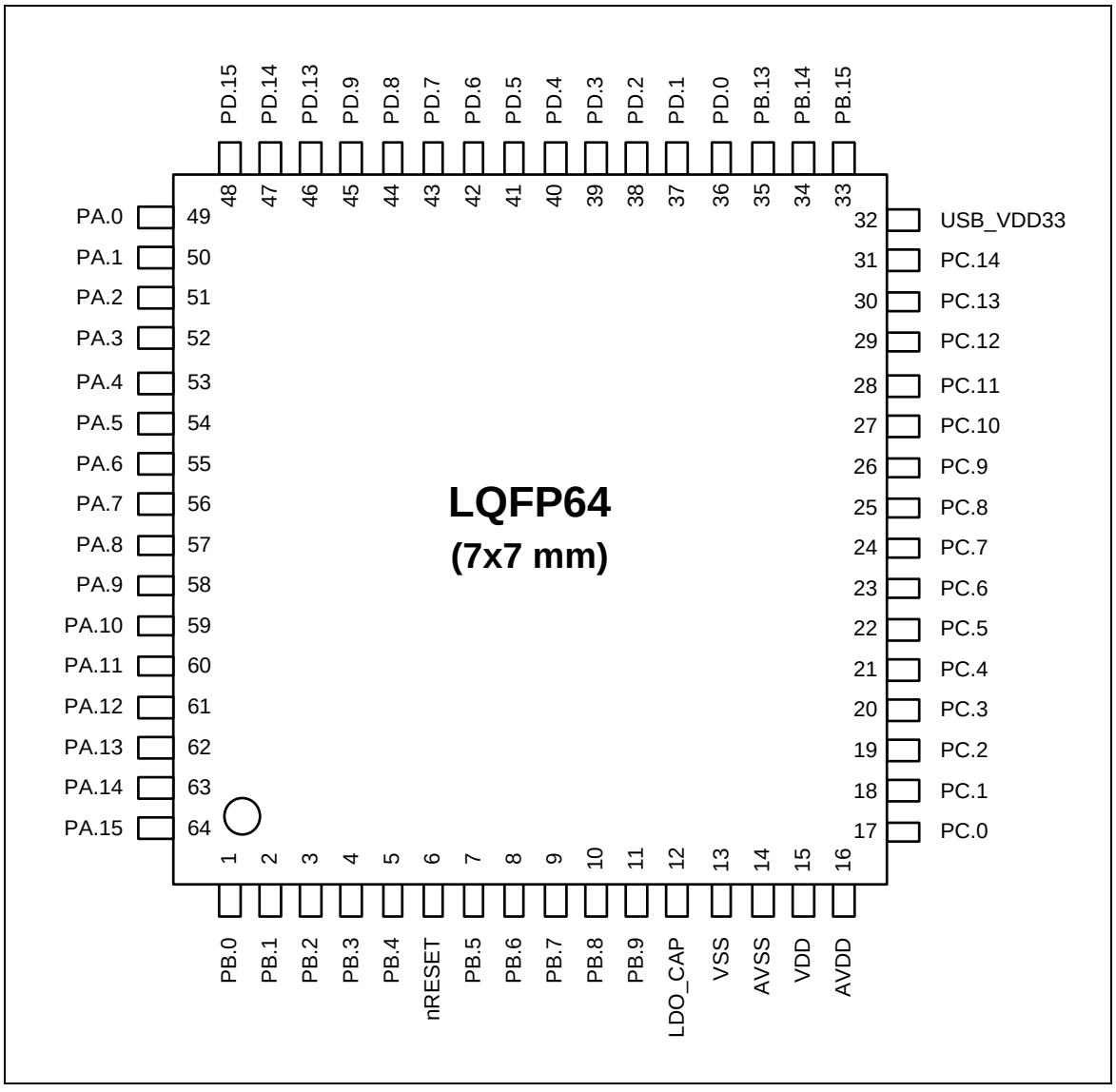


Figure 4.3-2 LQFP64 (7x7 mm) Pin Diagram

4.4 Pin Description

MFP = Multi-function pin.

Note: Pin Type I=Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
1	1	PB.0	I/O	MFP0	General purpose digital I/O pin.
		PWM0_SYNC_IN	I/O	MFP1	PWM0 counter synchronous trigger input pin.
		I2C0_SCL	I/O	MFP2	I2C0 clock pin.
		PWM0_CH0	I/O	MFP3	PWM0 channel0 output/capture input.
2	2	PB.1	I/O	MFP0	General purpose digital I/O pin.
		PWM0_SYNC_OUT	I/O	MFP1	PWM0 counter synchronous trigger output pin.
		I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
		PWM0_CH1	I/O	MFP3	PWM0 channel1 output/capture input.
3	3	PB.2	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH0	I/O	MFP1	PWM0 channel0 output/capture input.
		TM2	I/O	MFP2	Timer2 event counter input / toggle output.
		PWM0_CH2	I/O	MFP3	PWM0 channel2 output/capture input.
4	4	PB.3	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH1	I/O	MFP1	PWM0 channel1 output/capture input.
		TM2_EXT	I/O	MFP2	Timer2 external capture input.
		DMIC_DAT1	I	MFP3	Digital microphone channel 1 data input pin.
		UART0_RXD	I	MFP4	UART0 Data receiver input pin.
		PWM0_CH3	I/O	MFP5	PWM0 channel3 output/capture input.
5	5	PB.4	I/O	MFP0	General purpose digital I/O pin.
		UART0_nCTS	I	MFP1	Clear to Send input pin for UART0.
		PWM0_CH0	I/O	MFP2	PWM0 channel0 output/capture input.
		DMIC_CLK1	O	MFP3	Digital microphone channel 1 clock output pin.
		UART0_TXD	O	MFP4	UART0 data transmitter output pin.
		PWM0_CH4	I/O	MFP5	PWM0 channel4 output/capture input.
6	6	RESETN	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
7	7	PB.5	I/O	MFP0	General purpose digital I/O pin.
		XT1_OUT	I	MFP1	External 4~24.576 MHz (high speed) crystal output pin.
		PWM0_CH1	I/O	MFP2	PWM0 channel1 output/capture input.
		I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
		I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
		DMIC_DAT0	I	MFP5	Digital microphone channel 0 data input pin.

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
8	8	PB.6	I/O	MFP0	General purpose digital I/O pin.
		XT1_IN	I	MFP1	External 4~24.576 MHz (high speed) crystal input pin.
		PWM0_CH2	I/O	MFP2	PWM0 channel2 output/capture input.
		I2C0_SCL	I/O	MFP4	I2C0 serial clock pin.
		I2C1_SCL	I/O	MFP5	I2C1 serial clock pin.
		DMIC_CLK0	O	MFP6	Digital microphone channel 0 clock output pin.
	9	PB.7	I/O	MFP0	General purpose digital I/O pin.
		UART0_nRTS	O	MFP1	Request to Send output pin for UART0.
		PWM0_CH3	I/O	MFP2	PWM0 channel3 output/capture input.
	10	PB.8	I/O	MFP0	General purpose digital I/O pin.
		UART0_TXD	O	MFP1	UART0 Data transmitter output pin.
		PWM0_CH4	I/O	MFP2	PWM0 channel4 output/capture input.
	11	PB.9	I/O	MFP0	General purpose digital I/O pin.
		UART0_RXD	I	MFP1	UART0 Data receiver input pin.
		PWM0_CH5	I/O	MFP2	PWM0 channel5 output/capture input.
9	12	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
10	13	VSS	P	MFP0	Ground pin for digital circuit.
11	14	AVSS	P	MFP0	Ground pin for analog circuit.
12	15	VDD	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
13	16	AVDD	P	MFP0	Power supply for internal analog circuit.
14	17	PC.0	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SCL	I/O	MPF1	I2C1 clock pin.
		X32_OUT	O	MFP2	External 32.768 kHz (low-speed) crystal output pin.
		SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin; or I2S1 data output pin.
15	18	PC.1	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SDA	I/O	MFP1	I2C1 data input/output pin.
		X32_IN	I	MFP2	External 32.768 kHz (low-speed) crystal input pin.
		SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin; or I2S1 data input pin.
16	19	PC.2	I/O	MFP0	General purpose digital I/O pin.
		I2C1_SMBSUS	O	MFP1	I2C1 SMBus SMBSUS# pin (PMBus CONTROL pin)
		TM3	I/O	MFP2	Timer3 event counter input / toggle output.
		SPI1_CLK	I/O	MFP3	SPI1 Serial Clock pin; or I2S1 bit clock pin.
		PC.3	I/O	MFP0	General purpose digital I/O pin.

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
17	20	I2C1_SMBAL	O	MFP1	I2C1 SMBus SMBALERT# pin
		TM3_EXT	I/O	MFP2	Timer3 external capture input.
		SPI1_SS	I/O	MFP3	SPI1 slave select pin; or I2S1 left right channel clock pin.
18	21	PC.4	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH2	I/O	MFP1	PWM0 channel2 output/capture input.
		CLKO	O	MFP2	Clock Output pin.
		SPI1_I2SMCLK	O	MFP3	SPI1 I2S master clock output pin.
	22	PC.5	I/O	MFP0	General purpose digital I/O pin.
		INT1	I	MFP1	External interrupt1 input pin.
		SPI2_MOSI	I/O	MFP2	SPI2 MOSI (Master Out, Slave In) pin.
	23	PC.6	I/O	MFP0	General purpose digital I/O pin.
		INT2	I	MFP1	External interrupt2 input pin.
		SPI2_MISO	I/O	MFP2	SPI2 MISO (Master In, Slave Out) pin.
	24	PC.7	I/O	MFP0	General purpose digital I/O pin.
		SPI0_SS0	I/O	MFP1	1st SPI0 Slave Select pin
		SPI2_CLK	I/O	MFP2	SPI2 serial clock pin.
	25	PC.8	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MOSI1	I/O	MFP1	2nd SPI0 MOSI (Master Out, Slave In) pin.
		SPI2_SS	I/O	MFP2	SPI2 Slave Select pin.
	26	PC.9	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MISO1	I/O	MFP1	2nd SPI0 MISO (Master In, Slave Out) pin.
		SPI2_I2SMCLK	O	MFP2	SPI2 I2S master clock output pin
	27	PC.10	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MOSI0	I/O	MFP1	1st SPI0 MOSI (Master Out, Slave In) pin.
		PWM0_BRAKE0	I	MFP2	Brake input pin 0 of PWM0.
		DPWM_RN	O	MFP3	Audio DPWM right channel negative output pin.
	28	PC.11	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MISO0	I/O	MFP1	1st SPI0 MISO (Master In, Slave Out) pin.
		PWM0_BRAKE1	I	MFP2	Brake input pin 1 of PWM0.
		DPWM_RP	O	MFP3	Audio DPWM right channel positive output pin.
	29	PC.12	I/O	MFP0	General purpose digital I/O pin.
		SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
		DPWM_LN	O	MFP3	Audio DPWM left channel negative output pin.
	30	PC.13	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH3	I/O	MFP1	PWM0 channel3 output/capture input.

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
		I2C0_SCL	I/O	MFP2	I2C0 clock pin.
		DPWM_LP	O	MFP3	Audio DPWM left channel positive output pin.
	31	PC.14	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH4	I/O	MFP1	PWM0 channel4 output/capture input.
		I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
		DPWM_SN	O	MFP3	Audio DPWM sub-woofer channel negative output pin.
19	32	USB_VDD33	P	MFP0	Power supply for USB, DC 3.3V.
20	33	PB.15	I/O	MFP0	General purpose digital I/O pin.
		USB_VBUS	P	MFP1	Power supply from USB or HUB.
		I2S0_MCLK	O	MFP2	I2S0 master clock output pin.
21	34	PB.14	I/O	MFP0	General purpose digital I/O pin.
		USB_D-	A	MFP1	USB differential signal D-.
		I2S0_DO	O	MFP2	I2S0 data output pin.
22	35	PB.13	I/O	MFP0	General purpose digital I/O pin.
		USB_D+	A	MFP1	USB differential signal D+.
		I2S0_DI	I	MFP2	I2S0 data input pin.
23	36	PD.0	I/O	MFP0	General purpose digital I/O pin.
		INT3	I	MFP1	External interrupt3 input pin.
		I2C1_SCL	I/O	MFP2	I2C1 clock pin.
		I2C0_SCL	I/O	MFP3	I2C0 clock pin.
		I2S0_BCLK	I/O	MFP4	I2S0 bit clock pin.
		DPWM_LN	O	MFP5	Audio DPWM left channel negative output pin.
24	37	PD.1	I/O	MFP0	General purpose digital I/O pin.
		INT4	I	MFP1	External interrupt4 input pin.
		I2C1_SDA	I/O	MFP2	I2C1 data p input/output in.
		I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
		I2S0_LRCK	I/O	MFP4	I2S0 left right channel clock pin.
		DPWM_LP	O	MFP5	Audio DPWM left channel positive output pin.
25	38	PD.2	I/O	MFP0	General purpose digital I/O pin.
		TRACE_CLK	O	MFP1	TPIU for ETM Tx trace clock output pin.
		SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
		I2S0_MCLK	O	MFP3	I2S0 master clock output pin.
		I2C1_SCL	I/O	MFP4	I2C1 clock pin.
		TM0	I/O	MFP5	Timer0 event counter input / toggle output.
26	39	PD.3	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA0	O	MFP1	TPIU for ETM Tx trace data output bit0.

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
		SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
		I2S0_LRCK	I/O	MFP3	I2S0 left right channel clock pin.
		DMIC_CLK1	O	MFP4	Digital microphone channel 1 clock output pin.
		TM2	I/O	MFP5	Timer2 event counter input / toggle output.
27	40	PD.4	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA1	O	MFP1	TPIU for ETM Tx trace data output bit1.
		SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
		I2S0_DI	I	MFP3	I2S0 data input pin.
		DMIC_DAT1	I	MFP4	Digital microphone channel 1 data input pin.
		TM1	I/O	MFP5	Timer1 event counter input / toggle output.
28	41	PD.5	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA2	O	MFP1	TPIU for ETM Tx trace data output bit2.
		SPI1_SS	I/O	MFP2	SPI1 Slave Select pin.
		I2S0_DO	O	MFP3	I2S0 data output pin.
		DMIC_CLK0	O	MFP4	Digital microphone channel 0 clock output pin.
		DPWM_RN	O	MFP5	Audio DPWM right channel negative output pin.
	42	PD.6	I/O	MFP0	General purpose digital I/O pin.
		TRACE_DATA3	O	MFP1	TPIU for ETM Tx trace data output bit3.
		SPI1_I2SMCLK	O	MFP2	SPI1 I2S master clock output pin
		I2S0_BCLK	I/O	MFP3	I2S0 Bit Clock pin.
		DMIC_DAT0	I	MFP4	Digital microphone channel 0 data input pin.
		DPWM_RP	O	MFP5	Audio DPWM right channel positive output pin.
	43	PD.7	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH5	I/O	MFP1	PWM0 channel5 output/capture input.
		INT1	I	MFP2	External interrupt1 input pin.
29	44	PD.8	I/O	MFP0	General purpose digital I/O pin.
		ICE_CLK	I	MFP1	Serial wired debugger clock pin
		TM0	I/O	MFP2	Timer0 event counter input / toggle output.
		I2C1_SCL	I/O	MFP3	I2C1 clock pin.
		I2C0_SCL	I/O	MFP4	I2C0 clock pin.
		DPWM_SN	O	MFP5	Audio DPWM sub-woofer channel negative output pin.
30	45	PD.9	I/O	MFP0	General purpose digital I/O pin.
		ICE_DAT	I/O	MFP1	Serial wired debugger data pin
	46	PD.13	I/O	MFP0	General purpose digital I/O pin.
		SPI0_SS1	O	MFP1	2nd SPI0 Slave Select pin

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
		EADC0_CH10	A	MFP2	EADC0 channel10 analog input.
31	47	PD.14	I/O	MFP0	General purpose digital I/O pin.
		UART0_nCTS	I	MFP1	Clear to Send input pin for UART0.
		EADC0_CH11	A	MFP2	EADC0 channel11 analog input.
		I2C0_SCL	I/O	MFP3	I2C0 clock pin.
		UART0_TXD	O	MFP4	UART0 data transmitter output pin.
		I2C1_SCL	I/O	MFP5	I2C1 clock pin.
32	48	PD.15	I/O	MFP0	General purpose digital I/O pin.
		UART0_nRTS	O	MFP1	Request to Send output pin for UART0.
		EADC0_CH12	A	MFP2	EADC0 channel12 analog input.
		I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
		UART0_RXD	I	MFP4	UART0 data receiver input pin.
		I2C1_SDA	I/O	MFP5	I2C1 data input/output pin.
33	49	PA.0	I/O	MFP0	General purpose digital I/O pin.
		SPI0_SS1	O	MFP1	2nd SPI0 Slave Select pin
		EADC0_CH0	A	MFP2	EADC0 channel0 analog input.
		DMIC_DAT0	I	MFP3	Digital microphone channel 0 data input pin.
34	50	PA.1	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MOSI1	I/O	MFP1	2nd SPI0 MOSI (Master Out, Slave In) pin.
		EADC0_CH1	A	MFP2	EADC0 channel1 analog input.
		DMIC_CLK0	O	MFP3	Digital microphone channel 0 clock output pin.
35	51	PA2	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MISO1	I/O	MFP1	2nd SPI0 MISO (Master In, Slave Out) pin.
		EADC0_CH2	A	MFP2	EADC0 channel2 analog input.
		DMIC_DAT1	I	MFP3	Digital microphone channel 1 data input pin.
36	52	PA.3	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MOSI0	I/O	MFP1	1st SPI0 MOSI (Master Out, Slave In) pin.
		EADC0_CH3	A	MFP2	EADC0 channel3 analog input.
		DMIC_CLK1	O	MFP3	Digital microphone channel 1 clock output pin.
37	53	PA.4	I/O	MFP0	General purpose digital I/O pin.
		SPI0_MISO0	I/O	MFP1	1st SPI0 MISO (Master In, Slave Out) pin.
		EADC0_CH4	A	MFP2	EADC0 channel4 analog input.
		DPWM_LN	O	MFP3	Audio DPWM left channel negative output pin.
38	54	PA.5	I/O	MFP0	General purpose digital I/O pin.
		SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
		EADC0_CH5	A	MFP2	EADC0 channel5 analog input.
		DPWM_LP	O	MFP3	Audio DPWM left channel positive output pin.
39	55	PA.6	I/O	MFP0	General purpose digital I/O pin.
		SPI0_SS0	I/O	MFP1	1st SPI0 Slave Select pin
		EADC0_CH6	A	MFP2	EADC0 channel6 analog input.
40	56	PA.7	I/O	MFP0	General purpose digital I/O pin.
		UART0_TXD	O	MFP1	UART0 data transmitter output pin.
		EADC0_CH7	A	MFP2	EADC0 channel7 analog input.
		SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin; or I2S2 data input pin.
41	57	PA.8	I/O	MFP0	General purpose digital I/O pin.
		UART0_RXD	I	MFP1	UART0 data receiver input pin..
		EADC0_CH8	A	MFP2	EADC0 channel8 analog input.
		SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin; or I2S2 data output pin.
42	58	PA.9	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SCL	I/O	MFP1	I2C0 Serial Clock pin
		EADC0_CH9	A	MFP2	EADC0 channel9 analog input.
		SPI2_SS	I/O	MFP4	SPI2 slave select pin; or I2S2 left right channel clock pin.
43	59	PA.10	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SDA	I/O	MFP1	I2C0 data input/output pin.
		EADC0_ST	I	MFP2	EADC0 external trigger input.
		DPWM_RN	O	MFP3	Audio DPWM right channel negative output pin.
		SPI2_CLK	I/O	MFP4	SPI2 clock pin; or I2S2 bit clock pin.
44	60	PA.11	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SMBSUS	O	MFP1	I2C0 SMBus SMBSUS# pin (PMBus CONTROL pin)
		TM0	I/O	MFP2	Timer0 event counter input / toggle output.
		DPWM_RP	O	MFP3	Audio DPWM right channel positive output pin.
45	61	PA.12	I/O	MFP0	General purpose digital I/O pin.
		I2C0_SMBAL	O	MFP1	I2C0 SMBus SMBALERT# pin
		TM0_EXT	I/O	MFP2	Timer0 external capture input.
		SPI2_I2SMCLK	O	MFP4	SPI2 I2S master clock output pin.
46	62	PA.13	I/O	MFP0	General purpose digital I/O pin.
		CLKO	O	MFP1	Clock Output pin.
		INT0	I	MFP2	External interrupt0 input pin.
		DPWM_SN	O	MFP3	Audio DPWM sub-woofer channel negative output

Pins		Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)				
					pin.
		I2C1_SCL	I/O	MFP4	I2C1 clock pin.
47	63	PA.14	I/O	MFP0	General purpose digital I/O pin.
		SPI0_SS0	I/O	MFP1	1st SPI0 Slave Select pin
		TM1	I/O	MFP2	Timer1 event counter input / toggle output.
		DPWM_SP	O	MFP3	Audio DPWM sub-woofer channel positive output pin.
		I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
48	64	PA.15	I/O	MFP0	General purpose digital I/O pin.
		INT0	I	MFP1	External interrupt0 input pin.
		TM1_EXT	I/O	MFP2	Timer1 external capture input.

Note:

1. Part number NPCA121DY do not provide DPWM and DMIC functionality.

Table 4.4-1 Pin Description

4.5 GPIO Alternate Function Summary

MFP* = Multi-function pin. (Reference section)

Pin function is defined in SYS_GPx_MFPx registers. For example PA0~7 pin functions are defined in SYS_GPA_MFPL register, and PA8~15 pin functions are defined in SYS_GPA_MFPH register.

MFP0	MFP1	MFP2	MFP3	MFP4	MFP5
PA.0	SPI0_SS1	EADC0_CH0	DMIC_DAT0		
PA.1	SPI0_MOSI1	EADC0_CH1	DMIC_CLK0		
PA.2	SPI0_MISO1	EADC0_CH2	DMIC_DAT1		
PA.3	SPI0_MOSI0	EADC0_CH3	DMIC_CLK1		
PA.4	SPI0_MISO0	EADC0_CH4	DPWM_LN		
PA.5	SPI0_CLK	EADC0_CH5	DPWM_LP		
PA.6	SPI0_SS0	EADC0_CH6			
PA.7	UART0_TXD	EADC0_CH7		SPI2_MISO	
PA.8	UART0_RXD	EADC0_CH8		SPI2_MOSI	
PA.9	I2C0_SCL	EADC0_CH9		SPI2_SS	
PA.10	I2C0_SDA	EADC0_ST	DPWM_RN	SPI2_CLK	
PA.11	I2C0_SMBSUS	TM0	DPWM_RP		
PA.12	I2C0_SMBAL	TM0_EXT		SPI2_I2SMCLK	
PA.13	CLKO	INT0	DPWM_SN	I2C1_SCL	
PA.14	SPI0_SS0	TM1	DPWM_SP	I2C1_SDA	
PA.15	INT0	TM1_EXT			
PB.0	PWM0_SYNC_IN	I2C0_SCL	PWM0_CH0		
PB.1	PWM0_SYNC_OUT	I2C0_SDA	PWM0_CH1		
PB.2	PWM0_CH0	TM2	PWM0_CH2		
PB.3	PWM0_CH1	TM2_EXT	DMIC_DAT1	UART0_RXD	PWM0_CH3
PB.4	UART0_nCTS	PWM0_CH0	DMIC_CLK1	UART0_TXD	PWM0_CH4
PB.5	XT1_OUT	PWM0_CH1	I2C0_SDA	I2C1_SDA	DMIC_DAT0
PB.6	XT1_IN	PWM0_CH2	I2C0_SCL	I2C1_SCL	DMIC_CLK0
PB.7	UART0_nRTS	PWM0_CH3			
PB.8	UART0_TXD	PWM0_CH4			
PB.9	UART0_RXD	PWM0_CH5			
PB.13	USB_D+	I2S0_DI			
PB.14	USB_D-	I2S0_DO			
PB.15	USB_VBUS	I2S0_MCLK			
PC.0	I2C1_SCL	X32_OUT	SPI1_MOSI		
PC.1	I2C1_SDA	X32_IN	SPI1_MISO		

MFP0	MFP1	MFP2	MFP3	MFP4	MFP5
PC.2	I2C1_SMBSUS	TM3	SPI1_CLK		
PC.3	I2C1_SMBAL	TM3_EXT	SPI1_SS		
PC.4	PWM0_CH2	CLKO	SPI1_I2SMCLK		
PC.5	INT1	SPI2_MOSI			
PC.6	INT2	SPI2_MISO			
PC.7	SPI0_SS0	SPI2_CLK			
PC.8	SPI0_MOSI1	SPI2_SS			
PC.9	SPI0_MISO1	SPI2_I2SMCLK			
PC.10	SPI0_MOSI0	PWM0_BRAKE0	DPWM_RN		
PC.11	SPI0_MISO0	PWM0_BRAKE1	DPWM_RP		
PC.12	SPI0_CLK		DPWM_LN		
PC.13	PWM0_CH3	I2C0_SCL	DPWM_LP		
PC.14	PWM0_CH4	I2C0_SDA	DPWM_SN		
PD.0	INT3	I2C1_SCL	I2C0_SCL	I2S0_BCLK	DPWM_LN
PD.1	INT4	I2C1_SDA	I2C0_SDA	I2S0_LRCK	DPWM_LP
PD.2	TRACE_CLK	SPI1_MOSI	I2S0_MCLK	I2C1_SCL	TM0
PD.3	TRACE_DATA0	SPI1_MISO	I2S0_LRCK	DMIC_CLK1	TM2
PD.4	TRACE_DATA1	SPI1_CLK	I2S0_DI	DMIC_DAT1	TM1
PD.5	TRACE_DATA2	SPI1_SS	I2S0_DO	DMIC_CLK0	DPWM_RN
PD.6	TRACE_DATA3	SPI1_I2SMCLK	I2S0_BCLK	DMIC_DAT0	DPWM_RP
PD.7	PWM0_CH5	INT1			
PD.8	ICE_CLK	TM0	I2C1_SCL	I2C0_SCL	DPWM_SN
PD.9	ICE_DAT	TM0_EXT	I2C1_SDA	I2C0_SDA	DPWM_SP
PD.13	SPI0_SS1	EADC0_CH10			
PD.14	UART0_nCTS	EADC0_CH11	I2C0_SCL	UART0_TXD	I2C1_SCL
PD.15	UART0_nRTS	EADC0_CH12	I2C0_SDA	UART0_RXD	I2C1_SDA

Table 4.5-1 GPIO Alternate Function Summary

5 BLOCK DIAGRAM

5.1 NPCA121 Series Block Diagram

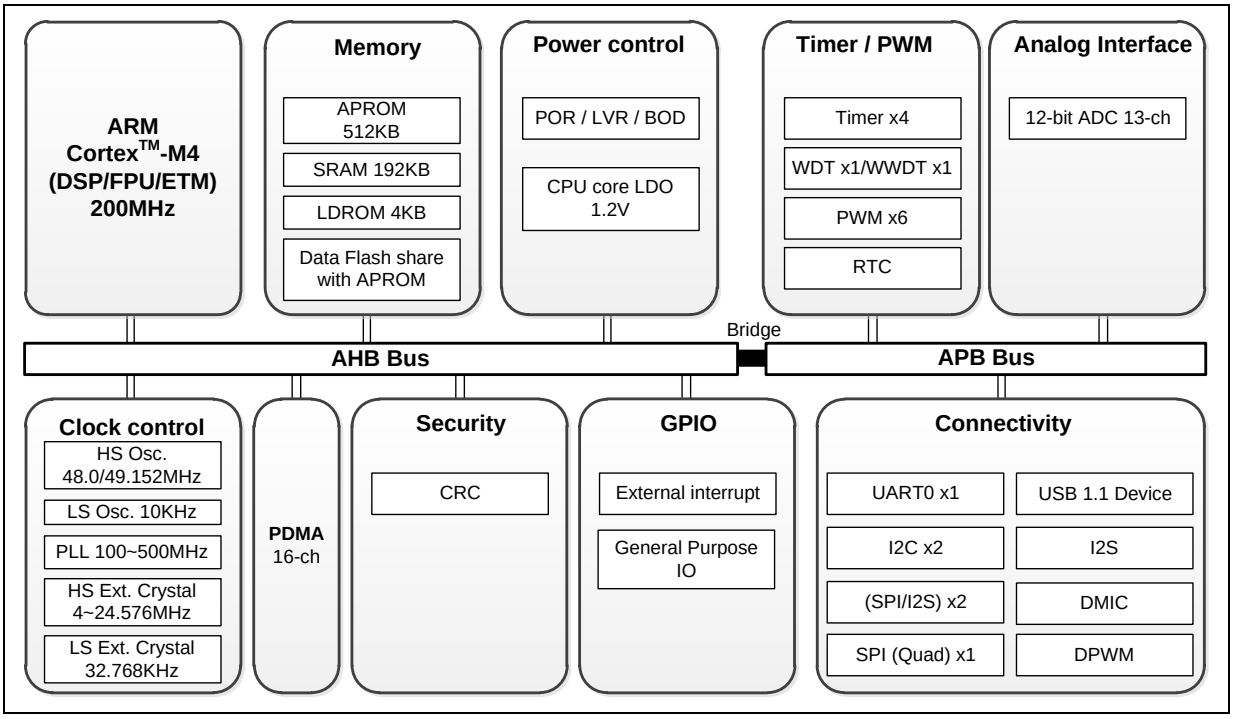


Figure 5.1-1 NPCA121 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NPCA121 series contains an embedded Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. The following figure shows the functional controller of the processor.

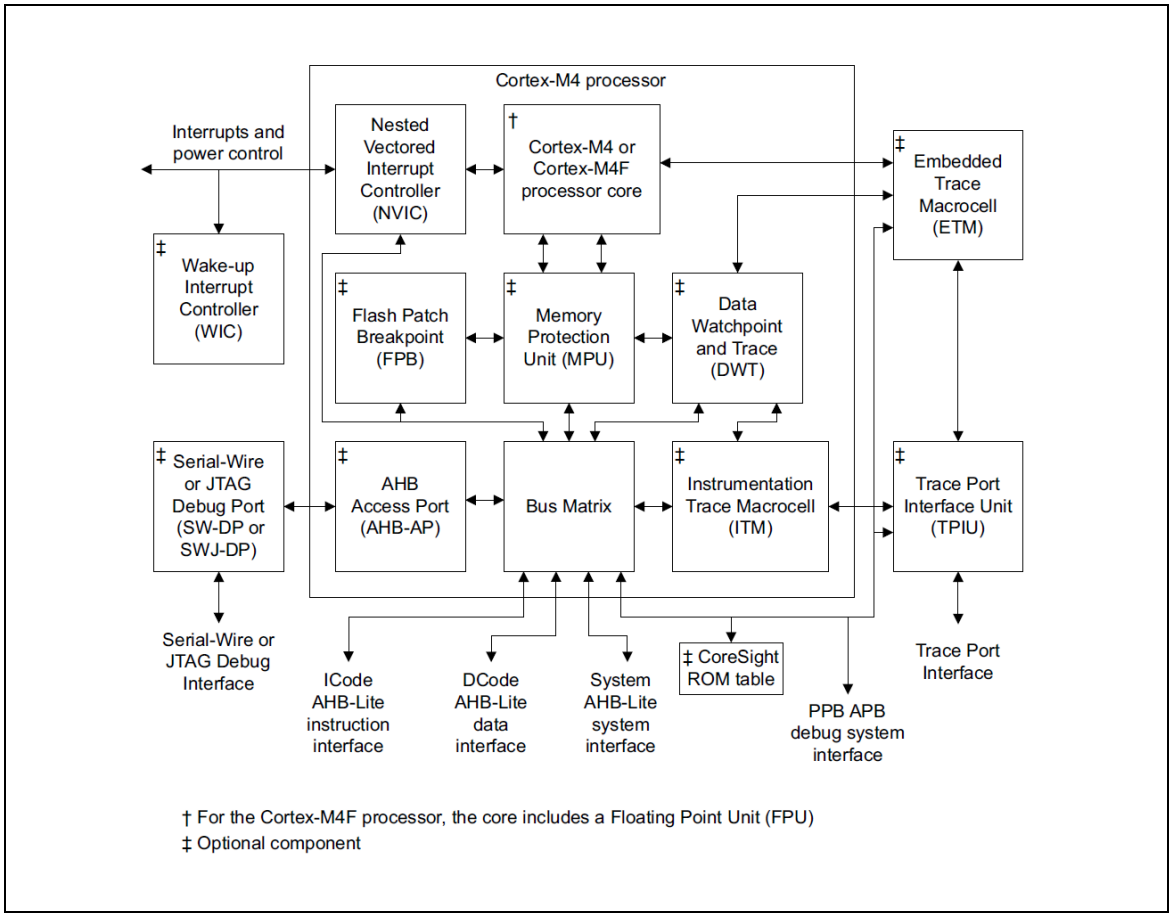


Figure 6.1-1 Cortex®-M4 Block Diagram

Cortex®-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)

- Hardware integer divide instructions, SDIV and UDIV
- Handler and Thread modes
- Thumb and Debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for ARMv6 big-endian byte-invariant or little-endian accesses
- Support for ARMv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NPCA121 series configured with 97 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and non-preempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.

- Serial Wire Debug Port(SW-DP) debug access
- Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

A system reset can be triggered by one of the nine sources listed below. The reset source can be identified by checking the reset flag bits in the System Reset Status Register (SYS_RSTSTS).

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset: writing 1 to CHIPRST (SYS_IPRST0[0]) will reset whole chip.
  - MCU Reset: writing 1 to SYSRESETREQ (AIRCR[2]) will reboot the device, according to the boot selection defined in configuration byte CONFIG0.
  - CPU Reset: writing 1 to CPURST (SYS_IPRST0[1]) will reset Cortex®-M4 core Only.

6.2.3 System Power Distribution

NPCA121 series device power distribution is divided into:

- Analog power from AV_{DD} and AV_{SS} : provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} : supplies the power to the internal regulator which provides a regulated 1.2 V power for digital operation.
- USB transceiver power from USB_V_{DD33} offers the power for operating the USB transceiver.

Analog power (AV_{DD}) should be at the same voltage level as digital power (V_{DD}).
Both power supplies should have decoupling capacitors placed as close as possible to pins preferably with no via.
The outputs of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to LDO_CAP pin and returned directly to V_{SS}. The Figure 6.2-1 shows the power distribution of the NPCA121 series.

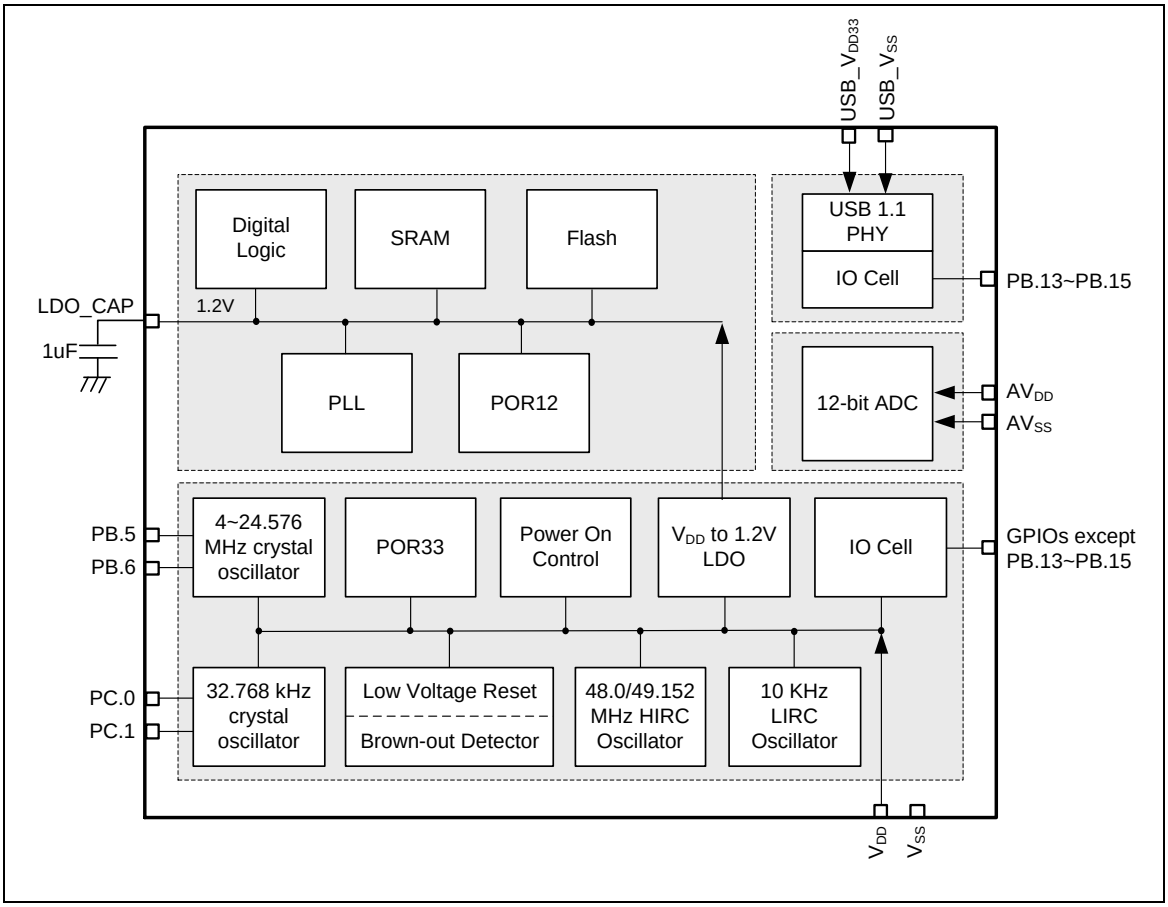


Figure 6.2-1 NPCA121 Series Power Distribution Diagram

6.2.4 System Memory Map

The NPCA121 series provides 4G-byte addressing space. The memory addresses assigned to each on-chip controllers are shown in Table 6.2.4-1. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NPCA121 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512 Kbytes)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 Kbytes)
0x2000_8000 – 0x2002_FFFF	SRAM1_BA	SRAM Memory Space (160 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers

0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I^2S0 Interface Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	PWM0_BA	PWM0 Control Registers
0x4006_0000 – 0x4006_0FFF	SPI0_BA	SPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI1_BA	SPI1 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI2_BA	SPI2 Control Registers
0x4006_3000 – 0x4006_30FF	DMIC_BA	DMIC Control Registers
0x4006_3100 – 0x4006_3FFF	VAD_BA	VAD Control Registers
0x4006_4000 – 0x4006_4FFF	DPWM_BA	DPWM Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I^2C1 Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2.4-1 Address Space Assignments for On-Chip Controllers

6.2.5 SRAM Memory Organization

The NPCA121 series supports up to 192 KB of embedded SRAM and the SRAM organization is separated to two banks: SRAM bank0 and SRAM bank1. The SRAM bank0 supports parity error check to make sure chip operating more stable.

- Supports up to 192 KB of SRAM
- Supports byte / half word / word write
- Supports parity error check function for SRAM bank0
- Supports oversize response error

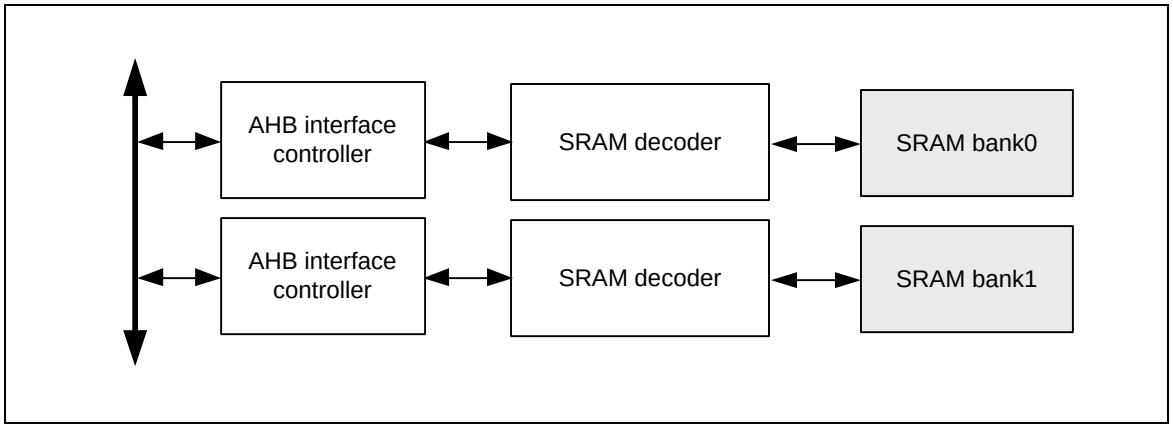


Figure 6.2-2 SRAM Block Diagram

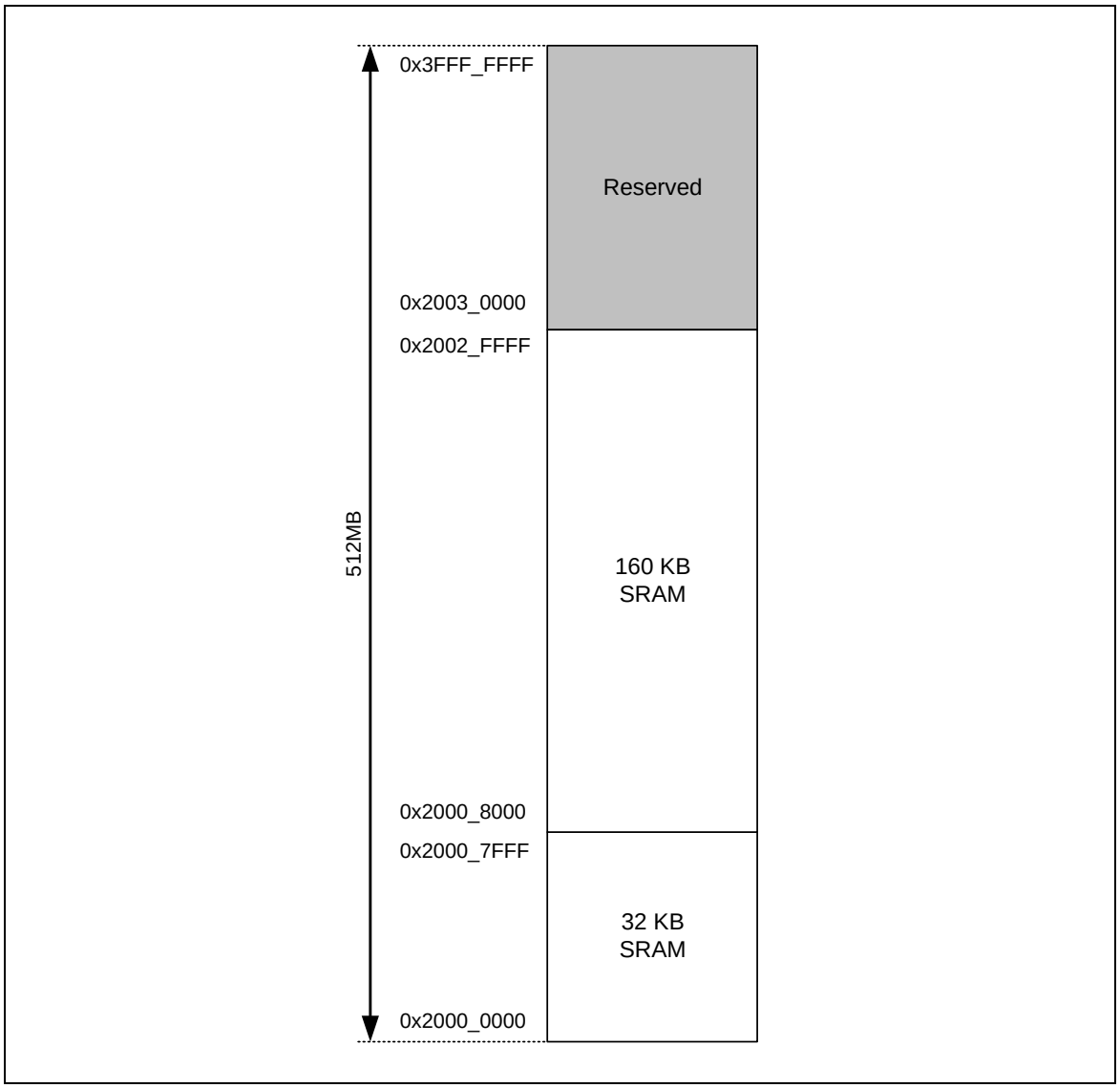


Figure 6.2-3 SRAM Memory Organization

SRAM address from 0x2000_0000 to 0x2000_7FFF has byte parity error check function. When CPU is accessing SRAM address from 0x2000_0000 to 0x2000_7FFF the parity error checking mechanism is operating dynamically. If parity error occurrs, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will record the address with parity error. Chip will enter interrupt when SRAM parity error occurs if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occurs, chip will stop detecting SRAM parity errors until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

6.2.6 System Timer (SysTick)

The Cortex®-M4 integrates a system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter decrements to zero, the COUNTFLAG status bit is set. A read or write on Current Value Register clears the COUNTFLAG bit to 0.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*ARM® Cortex™-M4 Technical Reference Manual*" and "*ARM® v6-M Architecture Reference Manual*".

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.
The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.7.1 Exception Model and System Interrupt Map

The Table 6.2.7-1 lists the exception model supported by NPCA121 Series. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.
When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,
The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Memory Manager Fault	4	0x00000010	Configurable
Bus Fault	5	0x00000014	Configurable
Usage Fault	6	0x00000018	Configurable
Reserved	7 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable

Reserved	13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 111	0x00000000 + (Vector Number)*4	Configurable

Table 6.2.7-1 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	SRAM_PERR	SRAM parity check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	Reserved	Reserved
22	6	RTC_INT	Real time clock interrupt
23	7	Reserved	Reserved
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt
27	11	EINT1	External interrupt
28	12	EINT2	External interrupt
29	13	EINT3	External interrupt
30	14	EINT4	External interrupt
31	15	EINT5	External interrupt
32	16	GPA_INT	External interrupt from PA[15:0] pin
33	17	GPB_INT	External interrupt from PB[14:12/9:0] pin
34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19	GPD_INT	External interrupt from PD[15:0] pin
36 ~ 37	20 ~ 21	Reserved	Reserved
38	22	SPI0_INT	SPI0 interrupt
39	23	SPI1_INT	SPI1 interrupt
40	24	BRAKE0_INT	PWM0 brake interrupt
41	25	PWM0_P0_INT	PWM0 pair 0 interrupt

42	26	PWM0_P1_INT	PWM0 pair 1 interrupt
43	27	PWM0_P2_INT	PWM0 pair 2 interrupt
44 ~ 47	28 ~ 31	Reserved	Reserved
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	Reserved	Reserved
54	38	I2C0_INT	I2C0 interrupt
55	39	I2C1_INT	I2C1 interrupt
56	40	PDMA_INT	PDMA interrupt
57	41	Reserved	Reserved
58	42	EADC0_INT	EADC interrupt source 0
59	43	EADC1_INT	EADC interrupt source 1
60	44	Reserved	Reserved
61	45	Reserved	Reserved
62	46	EADC2_INT	EADC interrupt source 2
63	47	EADC3_INT	EADC interrupt source 3
64 ~ 66	48~ 50	Reserved	Reserved
67	51	SPI2_INT	SPI2 interrupt
68	52	DMIC_INT	DMIC interrupt
69	53	USBD_INT	USB device interrupt
70 ~ 71	54 ~ 55	Reserved	Reserved
72	56	VAD_INT	VAD interrupt
73 ~ 77	57 ~ 61	Reserved	Reserved
78	62	DPWM_INT	DPWM interrupt
79 ~ 83	63 ~ 67	Reserved	Reserved
84	68	I2S0_INT	I^2S0 interrupt
85 ~ 111	69 ~ 95	Reserved	Reserved

Table 6.2.7-2 Interrupt Number Table

6.2.7.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until

cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.
NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.
NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).
The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M4 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24.576 MHz external high speed crystal (HXT) and internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The Figure 6.3-1 shows the clock generator and the overview of the clock source control.

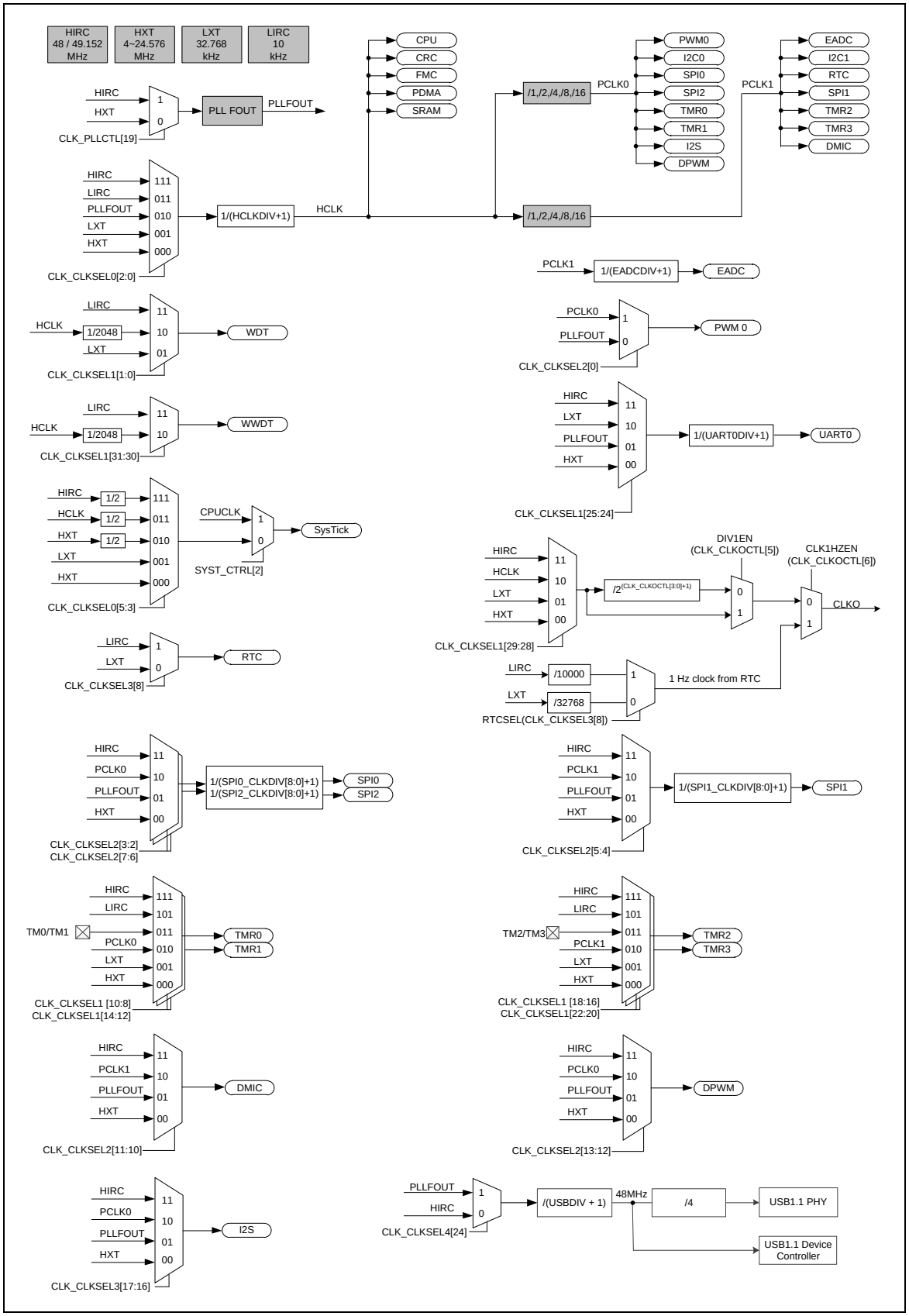


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

Five clock sources can be used to drive all the internal clocks:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24.576 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24.576 MHz external high speed crystal (HXT) or internal high speed oscillator (HIRC)
- Selectable 48.0 MHz or 49.152 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

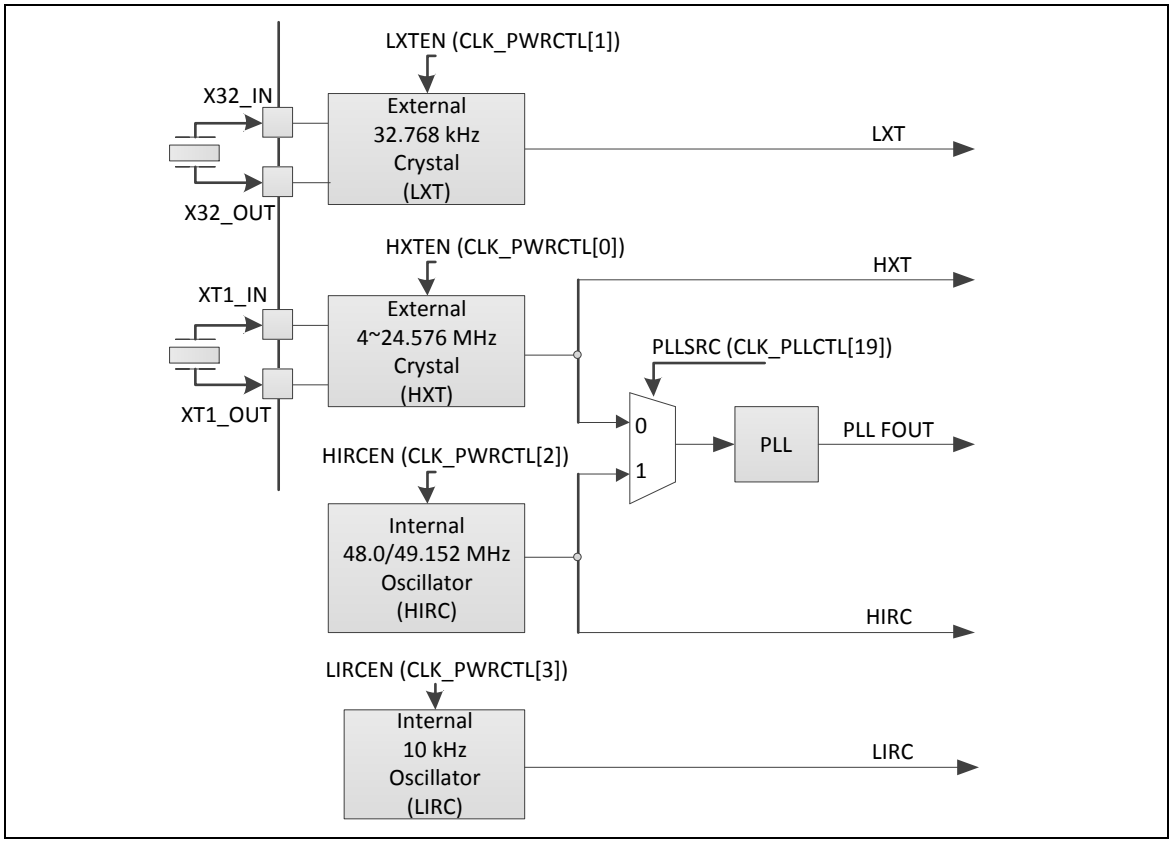


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

Five clock sources can be used to drive the system clock (HCLK), as shown in Figure 6.3-3. Clock source can be chosen by configuring HCLKSEL bits(CLK_CLKSEL0[2:0]).

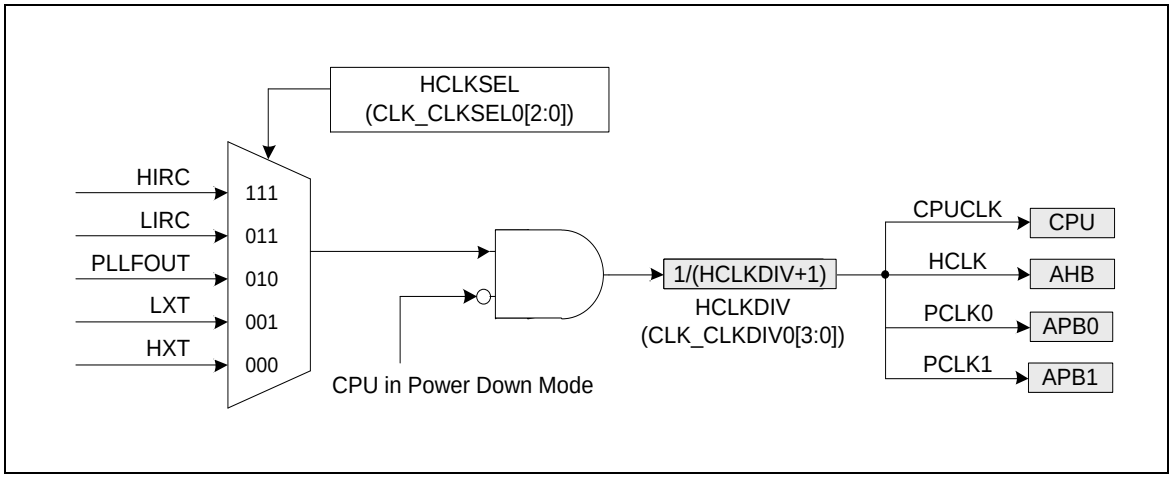


Figure 6.3-3 System Clock Block Diagram

There are two clock failure detectors monitoring HXT and LXT; each has its own enabling and interrupt control.

If HXT failure detector is enabled, the HIRC clock will be also enabled automatically. The clock controller will automatically switch the system clock (HCLK) source from HXT to HIRC if the following conditions are met:

- HCLK clock source was from HXT, or from PLLOUT and PLL source clock was from HXT,
- HXT clock failure has been detected.

An HXT clock failure condition will set HXTFIF bit (CLK_CLKDSTS[0]) 1, and raise an HXT failure interrupt if HXTFIEN (CLK_CLKDCTL[5]) is enabled.

To recover from HXT failure, user can first disable HXT, then enable HXT, and then check if the HXT clock stable bit HXTSTB (CLK_STATUS[0]) is 1. HXTSTB bit being 1 means HXT is recovered and enabled so that system clock source can be switched to HXT again.

The hardware procedure of HXT failure detection and system clock source auto switch to HIRC is shown in the Figure 6.3-4.

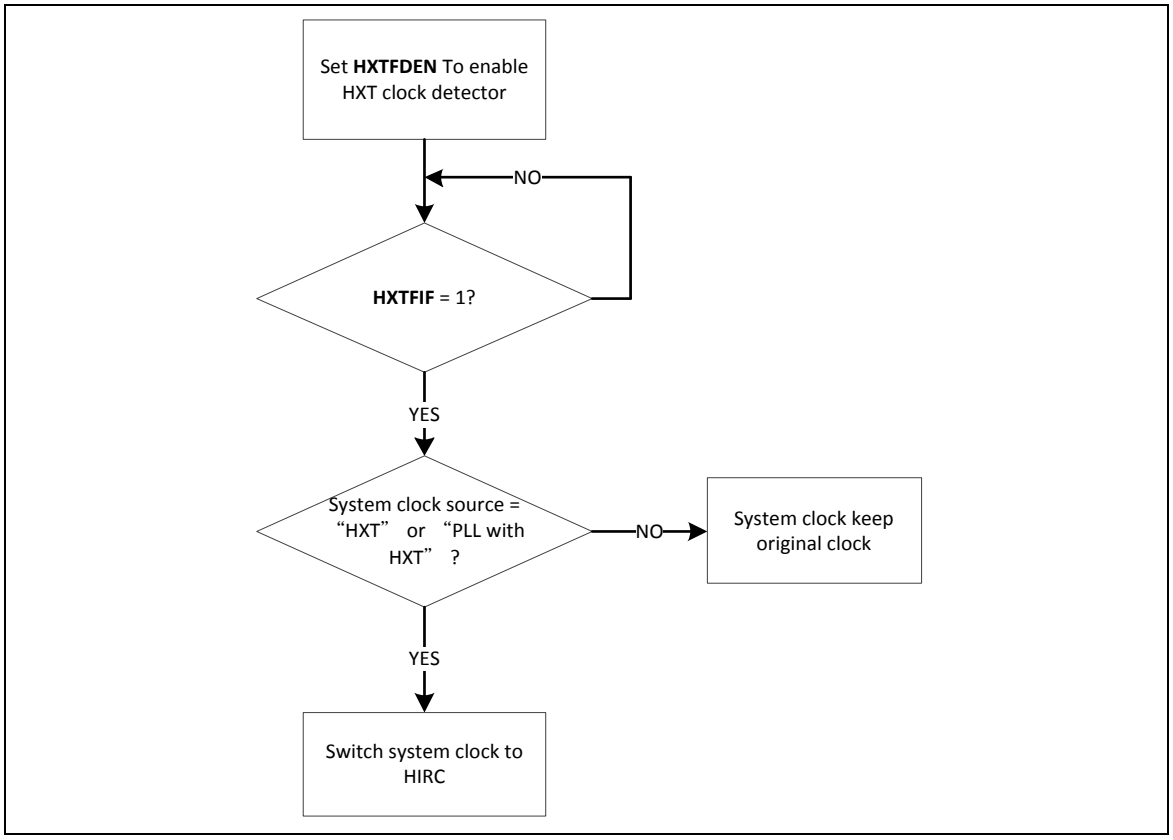


Figure 6.3-4 HXT Stop Protect Procedure

The SysTick clock source can be from CPU clock or external reference clock, determined by CLKSRC bit (SYST_CTRL[2]).

- If CLKSRC = 1, CPU core clock is used for SysTick,
- If CLKSRC = 0, SysTick clock source is from one of the 5 external reference clock, which is chosen by STCLKSEL bits (CLK_CLKSEL0[5:3]), shown in Figure 6.3-5.

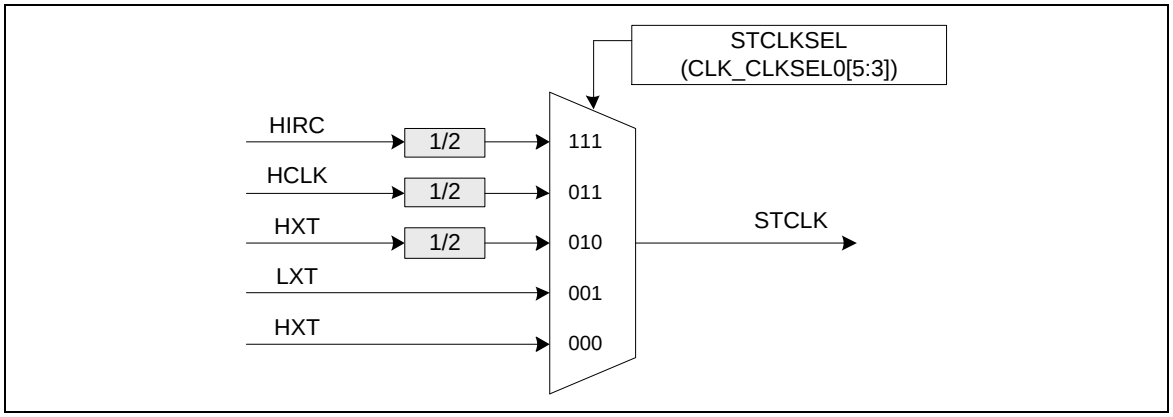


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripheral Clock

Each peripheral module can have its own clock source selection and configuration, please refer to

CLK_CLKSEL1 and CLK_CLKSEL2 register description for more detailed information.

6.3.5 Power-down Mode Clock

Different power down modes have different impact on the system clocks. Under a certain power down mode, some clock sources (including system clocks and peripheral clocks) are disabled while some other clock sources are still available. However regardless the power down mode the following clocks are always available:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripheral Clock which uses LXT or LIRC as clock source

6.3.6 Clock Output

The NPCA121 series device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

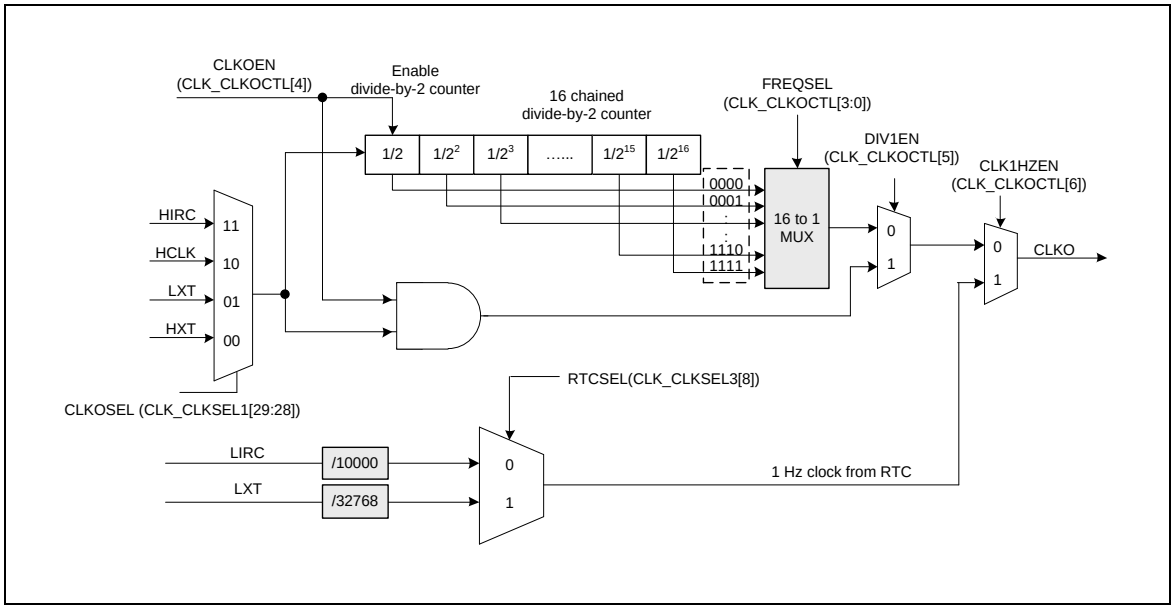


Figure 6.3-6 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NPCA121 Series provides up to 512 KB of on-chip embedded flash for application program memory (APROM) and data flash. In-System-Programming (ISP) and In-Application-Programming (IAP) enables user to update chip embedded flash when chip is soldered on PCB. After chip powers-on, Cortex®-M4 CPU fetches code from APROM or LDROM depending on the boot select (CBS) configuration in CONFIG0. The NPCA121 Series also provides Data Flash for user to store some application dependent data to be retained when chip is powered off.

The NPCA121 Series supports configurable data flash size. The data flash size is decided by data flash enable (DFEN) in CONFIG0 and data flash base address (DFBA) in CONFIG1. When DFEN is set to 1, the data flash size is zero. When DFEN is set to 0, the APROM and data flash share 512 KB continuous address and the start address of data flash is defined by (DFBA) in CONFIG1.

6.4.2 Features

- Supports up to 512 KB of application ROM (APROM).
- Supports 4 KB loader ROM (LDROM).
- Supports Data Flash with configurable memory size.
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 4 KB page erase for all embedded flash.
- Supports 32-bit/64-bit and multi-word flash programming function.
- Supports fast flash programming verification function.
- Supports CRC32 checksum calculation function.
- Supports flash all one verification function
- Supports cache memory to improve flash access performance and reduce power consumption.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory.
- Supports cache memory to improve flash access performance and reduce power consumption.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NPCA121 series device has up to 58 General Purpose I/O (GPIO) pins, grouped in 4 ports PA, PB, PC and PD. Port PA, PC and PD each has 16 pins, and there are 13 pins in Port PB.

All the GPIO pins are multi-functional pins, in that they can be I/O pins or they can work as alternate function pins. Each pin can be individually configured. Pin function are defined in MFP registers, for example PA0~7 pin functions are defined in SYS_GPA_MFPL register.

When working as an I/O pin, each pin can be configured by software in several modes:

- Input
- Push-pull Output
- Open-Drain Output
- Quasi-bidirectional

After a power-on or reset event, all GPIO pins' default working mode are determined by CIOINI bit (CONFIG0[10]) except PA.8. PA.8 pin default I/O mode is determined by GPA8_LOW bit (CONFIG0[11]). Every I/O pin has a weak pull-up resistor with value ~50 kΩ when I/O pin configured as quasi-bidirectional output low.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input capability
- I/O pin can be configured as interrupt source with edge/level trigger option
- Supports High Drive and High Slew Rate I/O mode
- CIOINI bit (CONFIG0[10]) configures all GPIO pins' default I/O mode except PA.8 after power-on or reset:
  - CIOINI = 0: Quasi-bidirectional mode,
  - CIOINI = 1: input mode.
- GPA8_LOW (CONFIG[11]) configures PA.8 pin's default I/O mode after power-on or reset:
  - GPA8_LOW = 0: Push-Pull mode and output low,
  - GPA8_LOW = 1: PA.8 follows CIOINI setting.
- I/O pin internal pull-up only available in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function
- PB0 ~ PB4, PB7 ~ PB9, PB13 ~ PB15, PC2 ~ PC15 and PD0 ~ PD15 support 5V-tolerance functions

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 16 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5

6.7 Timer Controller (TMR)

6.7.1 Overview

The Timer controller contains four 32-bit multi-functional timers, Timer0, 1, 2 and 3. These timers can be used to count, or time external events that drive the Timer input pins.

Or the four timers can be configured as four PWM generators; each can support two PWM output channels in independent or complementary mode. The output state of PWM output pin can be control by pin mask, polarity, and dead-time generator.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer equips one 24-bit up counter and one 8-bit prescaler counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and PDMA function
- Supports Inter-Timer trigger mode

6.7.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescaler
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
- Supports trigger ADC on the following events:

- PWM zero point, period, zero or period point, up-count compared or down-count compared point events

6.8 PWM Generator and Capture Timer (PWM)

6.8.1 Overview

The NPCA121 series provides one PWM generators – PWM0. It supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM using comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for EADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various PWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.8.2 Features

6.8.2.1 PWM function features

- Clock source supports maximum clock frequency up to 200 MHz
- Supports up to 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin, system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM counter match zero, period value or compared value
  - PWM counter match free trigger comparator compared value (only for EADC)

6.8.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.9.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip power-on or reset by setting CWDTEN[2:0] in CONFIG0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz or LXT.

6.10 Window Watchdog Timer (WWDT)

6.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.10.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.11 Real Time Clock (RTC)

6.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar message are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.11.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) setting in RTC_TALM and RTC_CALM
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensate by RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated

6.12 UART Interface Controller (UART)

6.12.1 Overview

The NPCA121 series is equipped with one Universal Asynchronous Receiver/Transmitters (UART) port, which offers a mean of full-duplex asynchronous communication with external device.

The NPCA121 series UART controller also supports RS-485 standard.

6.12.2 Features

- One UART port: UART0.
- Programmable baud-rate generator
- Separate receive (RX) and transmit (TX) FIFOs with 16 bytes each to reduce CPU interrupt service loading
- RX FIFO trigger level of 1/16, 4/16, 8/16 and 14/16.
- Supports hardware auto-flow control
- Supports wake-up function which can be triggered by nCTS, incoming data, RX FIFO reached threshold or RS-485 Address Match (AAD mode).
- Supports 8-bit RX FIFO time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - 5, 6, 7, or 8 data bits
  - even, odd, stick or no-parity generation/detection
  - 1, 1.5, or 2 stop bit generation
- Support PDMA transfer function
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - hardware or software managing nRTS pin to control RS-485 transmission direction

UART Feature	UART0
FIFO	16 Bytes
Auto Flow Control (CTS/RTS)	√
RS-485 Function Mode	√
nCTS Wake-up	√
Incoming Data Wake-up	√

RX FIFO reached threshold Wake-up	√
RS-485 Address Match (AAD mode) Wake-up	√
Auto-Baud Rate Measurement	√
STOP Bit Length	1, 1.5, 2 bit
Word Length	5, 6, 7, 8 bits
Even / Odd Parity	√
Stick Bit	√
√ = Supported	

Table 6.12.2-1 UART Feature

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The NPCA121 series device provides two sets of I²C controller which can function as either master or slave, provide multi-master capability, support up to 1Mbs transfer rate.

The NPCA121 I2C module can also be used for a variety of purposes, including CRC verification, SMBus (System Management Bus) and PMBus (Power Management Bus).

6.13.2 Features

The NPCA121 series I2C module supports the following features:

- Two I²C ports
- Master, Salve and Multi-master mode operation
- Support High speed mode 3.4Mbps
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- 7-bit and 10-bit addressing mode
- Multiple address recognition (four slave address with mask option)
- Power-down wake-up function
- PDMA capability with one buffer
- Programmable setup/hold time
- Bus Management (SM/PM compatible) function

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication interface. SPI devices communicate in full duplex mode using a master-slave architecture. The single master and the slave(s) communicate bi-directionally through a 4-wire interface.

The NPCA121 series contains up to three sets of SPI controllers which perform serial-to-parallel conversion when receiving data from a peripheral device, and parallel-to-serial conversion when transmitting data to a peripheral device. Each SPI controller can be configured as a master or a slave device.

SPI0 controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode. SPI1 and SPI2 controllers support I^2S mode to connect external audio CODEC. Each SPI controller supports the PDMA function to access the data buffer.

6.14.2 Features

- SPI Mode
  - Up to three sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 25 MHz and Slave mode up to 25 MHz (when chip works at VDD = 2.7~3.6V)
  - Supports 2-bit Transfer mode (SPI0 Only)
  - Supports Dual and Quad I/O Transfer mode (SPI0 Only)
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-/8-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface (SPI0 Only)
  - Supports one data channel half-duplex transfer
  - Support receive-only mode

- I^2S Mode (for SPI1~SPI2)
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

	SPI0	SPI1 / SPI2
Dual/Quad I/O Mode	V	X
Two-Bit Transfer Mode	V	X
FIFO Depth	8-level	SPI mode 8~16 bits data length: 8-level Otherwise: 4-level
Slave Time-out Function	V	X
Slave 3-Wired Mode	V	X
I^2S Mode	X	V

Table 6.14.2-1 SPI feature difference (SPI0~SPI2)

6.15 CRC Controller (CRC)

6.15.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with programmable polynomial settings.

6.15.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.16 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.16.1 Overview

The NPCA121 series contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 13 external input channels. The ADC converter can be started by software trigger, PWM0 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.16.2 Features

- Analog input voltage range: 0~AV_{DD}.
- Reference voltage from AVDD.
- 12-bit resolution and 9-bit accuracy is guaranteed.
- Up to 13 single-end analog external input channels.
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses.
- Maximum ADC clock frequency is 60 MHz.
- Up to 2 MSPS conversion rate.
- Configurable ADC internal sampling time.
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
- Supports calibration capability when EADC enabled.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode.
  - Standby mode.
- Up to 13 sample modules
  - Each of sample modules which is configurable for ADC converter channel EADC_CH0~12 and trigger source.
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module.
  - Conversion results are held in 13 data registers with valid and overrun indicators.
- An ADC conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n] , n = 0~12)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - PWM triggers
- Supports PDMA transfer

6.17 I²S Controller (I²S)

6.17.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively and is capable of handling 8/16/24/32 bits audio data sizes. PDMA controller handles the data movement between FIFO and memory.

6.17.2 Features

- Support Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.18 USB 1.1 Device Controller (USBD)

6.18.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1KBytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.18.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1KBytes buffer size
- Provides remote wake-up capability

6.19 Digital Microphone Inputs (DMIC)

6.19.1 Overview

Using the dual channel digital PDM (Pulse Density Modulation) microphone interface (DMIC_CLK0, DMIC_DAT0, DMIC_CLK1 and DMIC_DAT1 pins) that are handled four digital PDM microphone inputs. Both DMIC_DAT0 and DMIC_DAT1 inputs are able to handle two digital microphones by selecting them alternately for each half of the clock cycle.

6.19.2 Features

The digital microphone interface use two wires (DMIC_DATn and DMIC_CLKn) to receive information from digital microphones. The main features of DMIC includes:

- Provides one 32-level FIFO data buffers for receiving.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Supports PDMA transfer.
- Supports up to four channel digital microphones.
- Both digital PDM microphone inputs can be used simultaneously.

6.20 Voice Active Detection (VAD)

6.20.1 Overview

The Voice Active Detection (VAD) analyses the PCM data from DMIC channel 0, and it consists of a SINC filter, a biquad filter and a VAD module. The idea of the VAD is to calculate the short term power and long term power of the input signal, and then compare the short term power with the short term power threshold. Moreover, the deviation of the short term power and long term power can be calculated and compared with the threshold deviation. Based on these two results, which can determine if the input signal is voice or not.

VAD can be active during idle mode and therefore provide lowest power operation, compared with a software based implementation.

6.20.2 Features

- Configuration detect levels.
- Supports idle mode wake-up function.
- Supports auto switch DMIC path when CPU wake-up by VAD.
- Generates interrupt requests when voice detected.

6.21 Audio DPWM Modulator (DPWM)

6.21.1 Overview

The DPWM modulator is sigma-delta modulator which is for class D amplifer. NPCA121 series has 3 DPWM modulator and each one can provide 2 differential bits.

6.21.2 Features

- Differential Audio PWM Output (DPWM)
- Support left channel,right channel and sub-woofer channel.
- Support sample rates from 16~96kHz.
- Programeable biquad filter with 10 band
- PDMA data channel for streaming of PCM audio data.
- Support the single precision floating point for input data and BIQ coefficient

7 ELECTRICAL CHARACTERISTICS (INDUSTRIAL GRADE)

This section will describe the AC/DC characteristic for industrial grade parts. For automotive grade, the preliminary temperature range is -40℃ to 105℃.

7.1 Absolute Maximum Ratings

7.1.1 Voltage Characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+3.6	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
$\|V_{SS} – AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance GPIO	-	5.5	V
	Input voltage on any other pin[2]	-	V_{DD}	V

Note:

1. Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the life and reliability of the device.
2. Non 5V-tolerance PIN: PA0 ~ PA15, PB5, PB6, PC0 and PC1.

Table 7.1.1-1 Voltage characteristics

7.1.2 Current Characteristics

Symbol	Parameter	Min	Max	Unit
I_{DD}	Maximum Current into V_{DD}	-	200	mA
I_{SS}	Maximum Current out of V_{SS}	-	100	
I_{IO}	Maximum Current sunk by a I/O pin	-	20	
	Maximum Current sourced by a I/O pin	-	20	
	Maximum Current sunk by total I/O pins	-	100	
	Maximum Current sourced by total I/O pins	-	100	

Table 7.1.2-1 Current characteristics

7.1.3 Thermal Characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	

Table 7.1.3-1 Thermal characteristics

7.1.4 Electrostatic Discharge (ESD) Ratings

Symbol	Ratings	Max	Unit
V_{ESD}	ESD for Human Body Model (HBM)	4	kV

Note:

1. This is guaranteed by characterization results, not tested in production

Table 7.1.4-1 Electrostatic Discharge (ESD) Ratings

7.2 General Operating Conditions

(V_{DD} - V_{SS} = 1.8 ~ 3.3 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{HCLK}	Internal AHB Clock Frequency	-	-	200	MHz	
V_{DD}	Typical Operation Voltage	1.8[1]	-	3.3[1]	V	
AV_{DD}	Analong Operation Voltage	V_{DD}			V	
USB_V_{DD33}	USB Operation Voltage	3.0	-	3.6	V	
V_{LDO}	LDO Output Voltage		1.2		V	Normal mode
C_{LDO}	LDO Output Capacitance on LDO_CAP Pin	-	1	-	uF	

Note:

1. The limitation of V_{DD} operation voltage is 1.62V ~ 3.6V.

Table 7.2-1 General Operating Conditions

7.3 DC Electrical Characteristics

(V_{DD} - V_{SS} = 1.8 ~ 3.3 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD5}	Operating Current Normal Run Mode HCLK = 49.152 MHz while(1){} executed from flash	-	10	16	mA	V_{DD}	3.3 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD6}		-	8	12	mA	V_{DD}	3.3 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD7}		-	10	16	mA	V_{DD}	1.8 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD8}		-	8	12	mA	V_{DD}	1.8 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD5}	Operating Current Normal Run Mode HCLK =12 MHz while(1){} executed from flash	-	5	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD6}	Operating Current Normal Run Mode HCLK = 160 MHz while(1){} executed from flash	-	3.2	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD7}		-	4.8	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD8}		-	3	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD9}		-	31	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled
I_{DD10}		-	21	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Disabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD11}		-	30.5	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled
I_{DD12}		-	20.7	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160M
						All digital modules	Disabled
I_{DD9}	Operating Current Normal Run Mode HCLK = 200 MHz while(1){} executed from flash	-	39	-	mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{DD10}		-	26.6	-	mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled
I_{DD11}		-	38.5	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{DD12}		-	26.3	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD13}	Operating Current Normal Run Mode HCLK =4 MHz while(1){} executed from flash	-	3.5	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD14}		-	2.4	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD15}		-	3.2	-	mA	V_{DD}	1.8V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD16}		-	2	-	mA	V_{DD}	1.8V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE1}	Operating Current Idle Mode HCLK = 49.152 MHz	-	6.1	10	mA	V_{DD}	3.3V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE2}	Operating Current Idle Mode HCLK =12 MHz	-	2.8	6	mA	V_{DD}	3.3V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE3}		-	6.1	10	mA	V_{DD}	1.8V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE4}		-	2.8	6	mA	V_{DD}	1.8V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE5}		-	3.5	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE6}		-	2.3	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE7}	Operating Current Idle Mode HCLK =160 MHz	-	3.4	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE8}		-	2.1	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE9}		-	19.6	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled
I_{IDLE10}			8.5		mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Disabled
I_{IDLE11}		-	19.4	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE12}	Operating Current Idle Mode HCLK =200 MHz	-	8.3	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Disabled
I_{IDLE9}		-	24.9	-	mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{IDLE10}			10.6		mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled
I_{IDLE11}		-	24.5	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{IDLE12}		-	10.3	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.6	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IDLE14}		-	2	-	mA	V_{DD} 3.3V HXT_GM 4 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{IDLE15}		-	2.3	-	mA	V_{DD} 1.8V HXT_GM 4 MHz HIRC Disabled PLL Disabled All digital modules Enabled
I_{IDLE16}		-	1.7	-	mA	V_{DD} 1.8V HXT_GM 4 MHz HIRC Disabled PLL Disabled All digital modules Disabled
I_{PWD1}	Power-down Mode (PD)	-	700	3500	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD2}		-	700	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD1}	Low Leakage Power-down Mode (LLPD)	-	350	1500	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD2}		-	350	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD1}	Standby Current Power-down Mode (SPD0 SRAM retention)	-	25	70	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD2}		-	25	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD1}	Standby Current Power-down Mode (SPD1)	-	15	46	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD2}		-	15	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD1}	Deep Power-down Mode (DPD)	-	2	6	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on USB_VDD33 pin floating.
I_{PWD2}		-	2	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on USB_VDD33 pin floating.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{PWD3}		-	3.5	7.5	μA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD4}		-	3.5	-	μA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on
I_{LK}	Input Leakage Current	-1	-	+1	μA	V_{DD} = 3.6 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage (TTL input)	-0.3	-	0.8	V	V_{DD} = 3.3 V
		-0.3	-	0.6		V_{DD} = 1.8 V
V_{IH1}	Input High Voltage (TTL input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 3.3 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 1.8 V
V_{ILS}	Negative going threshold (Schmitt input), nRESET	-0.3	-	0.3 V_{DD}	V	
V_{IHS}	Positive going threshold (Schmitt input), nRESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	
R_{RST}	Internal nRESET pin pull up resistor	-	50	-	kΩ	
V_{ILS}	Schmitt input high voltage		0.6* V_{DD}	0.75* V_{DD}	V	
V_{IHS}	Schmitt input low voltage	0.3* V_{DD}	0.4* V_{DD}		V	
Hysteresis	Schmitt buffer hysteresis	-	0.2 V_{DD}	-	V	
I_{SR11}	Source Current (Quasi-bidirectional Mode)	-	-9.3	-	μA	V_{DD} = 3.3 V, V_S = 2.8 V
I_{SR12}		-	-7.5	-	μA	V_{DD} = 2.7 V, V_S = 2.3 V
I_{SR13}		-	-5.6	-	μA	V_{DD} = 1.8 V, V_S = 1.5 V
I_{SR21}	Source Current (Push-pull Mode)	-	-20	-	mA	V_{DD} = 3.3 V, V_S = 2.8 V
I_{SR22}		-14	-15	-	mA	V_{DD} = 2.7 V, V_S = 2.3 V
I_{SR23}		-11	-7.9	-	mA	V_{DD} = 1.8 V, V_S = 1.5 V
I_{SK11}	Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode)	14	20	-	mA	V_{DD} = 3.3 V, V_S = 0.5 V
I_{SK12}		11	15	-	mA	V_{DD} = 2.7 V, V_S = 0.4 V
I_{SK13}		-	8.2	-	mA	V_{DD} = 1.8 V, V_S = 0.3 V

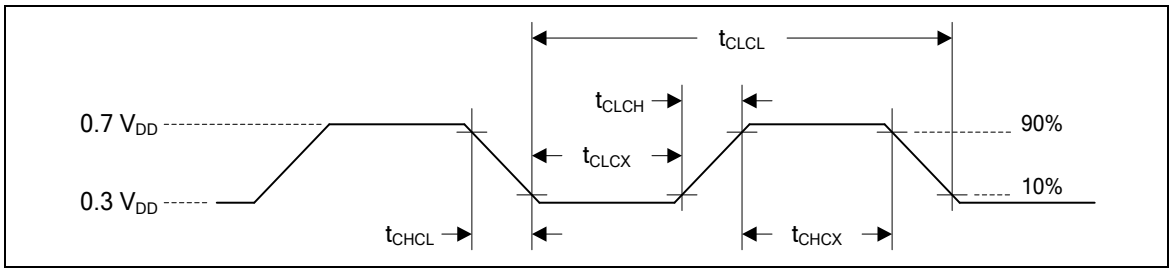
Notes:

1. nRESET pin is a Schmitt trigger input.

Table 7.3-1 DC Electrical Characteristics

7.4 AC Electrical Characteristics

7.4.1 External High Speed Crystal (HXT) Characteristics



Note:

1. Duty cycle is 50%.
2. Guaranteed by design, not tested in production

Figure 7.4-1 External High Speed Crystal Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

Table 7.4.1-1 External High Speed Clock Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{HXT}	Operation Temperature	-40	25	85	℃	-
f_{HXT}	Oscillator Frequency	4	12	24.576	MHz	
I_{HXT}	Operating Current	-	0.37	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 4 MHz T_A = 25 ℃, GM TYPE
		-	0.5	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 12 MHz T_A = 25 ℃, GM TYPE
		-	0.66	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 16 MHz T_A = 25 ℃, GM TYPE
		-	0.84	-	mA	V_{DD} = 3.3V, f_{HXTAL} =24 MHz T_A = 25 ℃, GM TYPE
		-	0.57	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 4 MHz T_A = 25 ℃, INV TYPE
		-	1.4	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 12 MHz T_A = 25 ℃, INV TYPE
		-	2.1	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 16 MHz T_A = 25 ℃, INV TYPE
		-	2.8	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 24 MHz

						T_A = 25 ℃, INV TYPE

Note:

1. This table is guaranteed by characteristics result, not tested in production.

Table 7.4.1-2 External High Speed Crystal (HXT) Characteristics

7.4.1.1 HXT Typical Crystal Application Circuit

CRYSTAL	C_1	C_2
4 MHz ~ 24.576 MHz	Optional (depending on the crystal specification)	

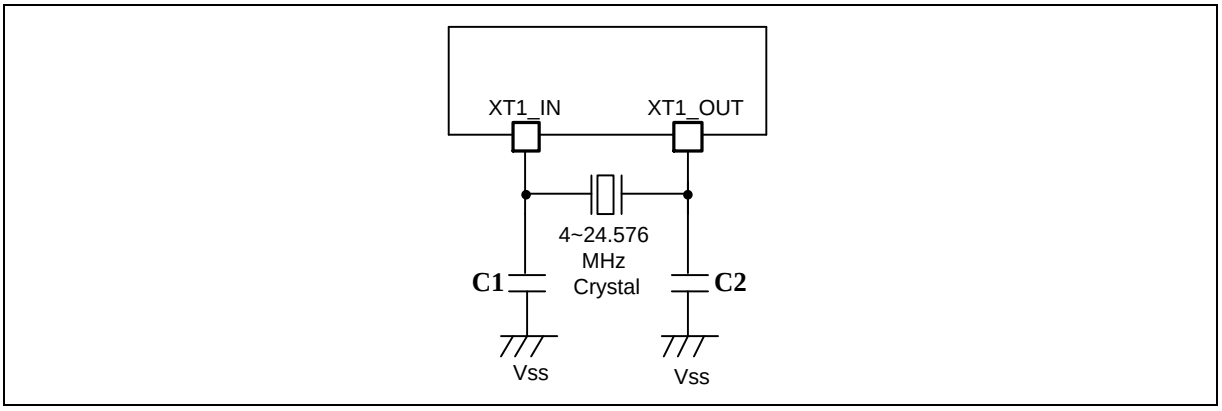


Figure 7.4-2 HXT Typical Crystal Application Circuit

7.4.2 Internal High Speed RC Oscillator (HIRC) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{HRC}	Operation Temperature	-40	25	85	℃	-
f_{HRC}	Center Frequency	-	49.152		MHz	-
	Calibrated Internal Oscillator Frequency	-	±0.25	-	%	T_A = 25 ℃ V_{DD} = 3.3 V
		-2	-	+2	%	T_A = -40℃~ 85 ℃
I_{HRC}	Operating Current	-	200	-	μA	T_A = 25 ℃,V_{DD} = 3.3 V

Table 7.4.2-1 Internal High Speed RC Oscillator (HIRC) Characteristics

7.4.3 External Low Speed Crystal (LXT) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{LXT}	Operation Temperature	-40	25	85	℃	-
f_{LXT}	Oscillator Frequency	-	32.768		kHz	
I_{LXT}	Operating Current	-	0.8	-	μA	T_A = 25 ℃,V_{DD} = 3.3 V

T_S	Stable Time		300	500	ms	

Table 7.4.3-1 External Low Speed Crystal (LXT) Characteristics

7.4.3.1 LXT Typical Crystal Application Circuit

CRYSTAL	C_1	C_2
32.768 kHz	Optional (depending on the crystal specification)	

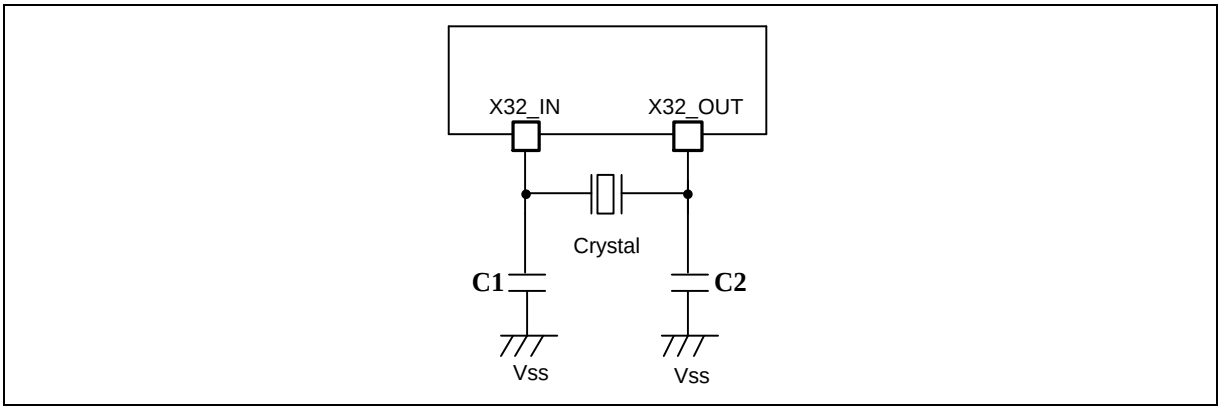


Figure 7.4-3 LXT Typical Crystal Application Circuit

7.4.4 Internal Low Speed RC Oscillator (LIRC) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{LRC}	Operation Temperature	-40	25	85	℃	-
f_{LRC}	Center Frequency	5	10	15	KHz	-
I_{LRC}	Operating Current	-	500	-	nA	T_A = 25 ℃, V_{DD} = 3.3 V

Table 7.4.4-1 Internal Low Speed RC Oscillator (LIRC) Characteristics

7.5 Analog Characteristics

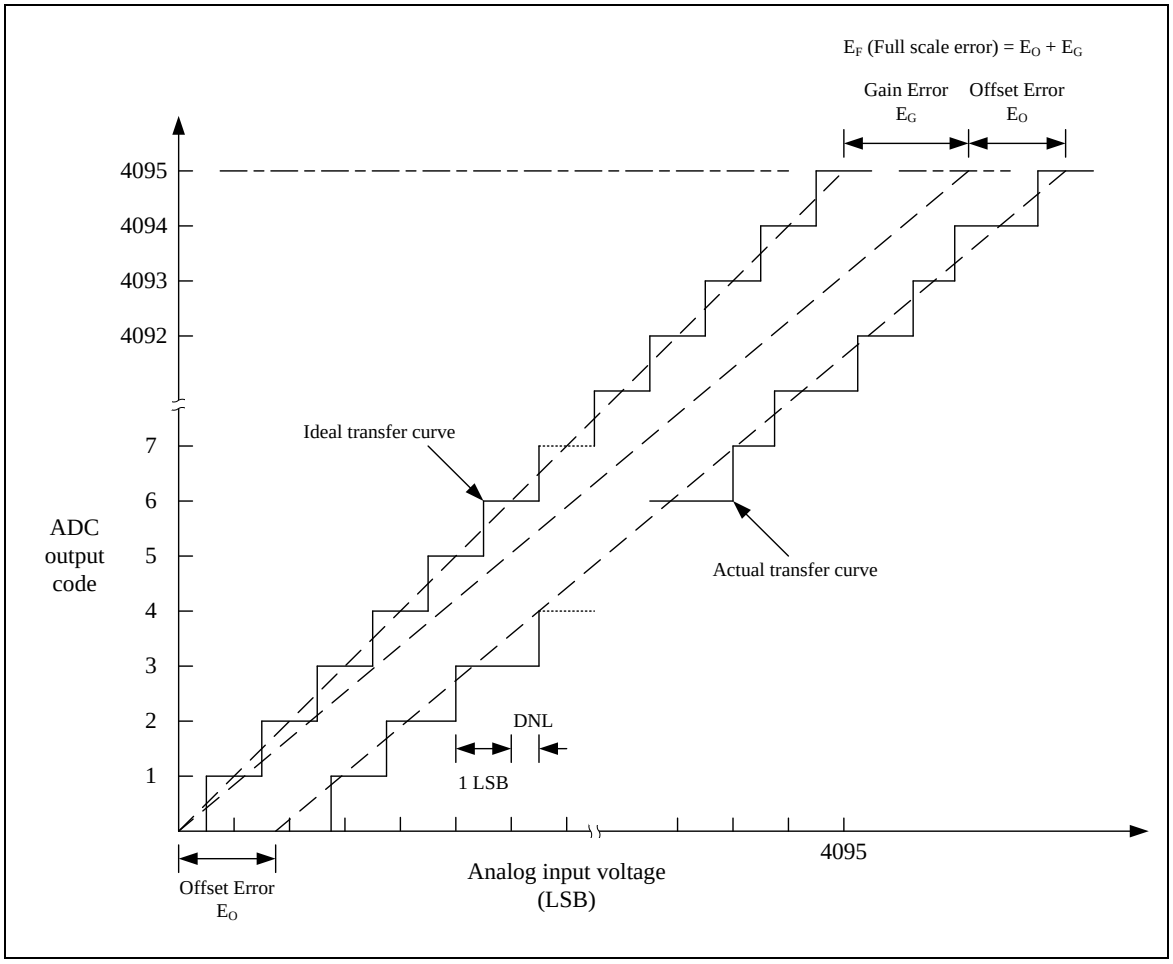
7.5.1 12-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution		12		Bit	-
DNL	Differential Nonlinearity Error	-	-	±2	LSB	2MSPS
INL	Integral Nonlinearity Error	-	-	±4	LSB	2MSPS
E_O	Offset Error	-	2	-	LSB	2MSPS
E_G	Gain Error (Transfer Gain)	-	-3	-	LSB	2MSPS
E_A	Absolute Error	-	6	-	LSB	2MSPS
-	Monotonic		Guaranteed		-	-
F_{ADC}	ADC Clock Frequency	0.14	-	60	MHz	AV_{DD} = 1.8~3.6 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	2000	kSPS	AV_{DD} = 1.8~3.6 V
T_{ACQ}	Acquisition Time (Sample Stage)		2~9		$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time		16~23		$1/F_{ADC}$	-
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	6	-	pF	-

Note:

1. This table is guaranteed by characteristics result, not tested in production.
2. The condition is that the error in a conversion started after ADC enable is less than ±0.5 LSB. The reference and input signal are already settled.

Table 7.5.1-1 12-bit SARADC Characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.5.2 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{LDO1}	Output Voltage	1.176	1.2	1.224	V	Normal mode
V_{LDO2}	Output Voltage		0.9		V	Low power mode
V_{LDO3}	Output Voltage		1.26		V	Over voltage mode

Notes:

1. It is critical that a 0.1 µF capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. To ensure power stability, a 1uF capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

Table 7.5.2-1 LDO Characteristics

7.5.3 Low Voltage Reset and Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
I_{BOD}	Operating Current	-	60		µA	V_{DD} = 3.6V
V_{BOD_F}	Brown-out Detect Level (Falling edge)	1.50	1.60	1.70	V	BODVL [2:0]=000
		1.70	1.80	1.90	V	BODVL [2:0]=001
		1.90	2.00	2.10	V	BODVL [2:0]=010
		2.10	2.20	2.30	V	BODVL [2:0]=011
		2.30	2.40	2.50	V	BODVL [2:0]=100
		2.50	2.60	2.70	V	BODVL [2:0]=101
		2.70	2.80	2.90	V	BODVL [2:0]=110
		2.90	3.00	3.10	V	BODVL [2:0]=111
V_{BOD_R}	Brown-out Detect Level (Rising edge)	-	V_{BOD_F} + V_{HYS_BOD}	-		
V_{HYS_BOD}	Hysteresis	-	80	-	mV	-
V_{LVR}	Low Voltage Reset Voltage	1.45	1.5	1.55	V	-

Table 7.5.3-1 Low Voltage Reset and Brown-out Detector Characteristics

7.5.4 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Power-on Reset Voltage		1.45		V	-
V_{PORHYS}	Power-on Reset Hysteresis	-	110	-	mV	-

RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	0.01	-	-	ms/V	-
FR_{VDD}	VDD Falling Rate to Ensure Power-on Reset	0.5	-	-	ms/V	-

Table 7.5.4-1 Power-on Reset Characteristics

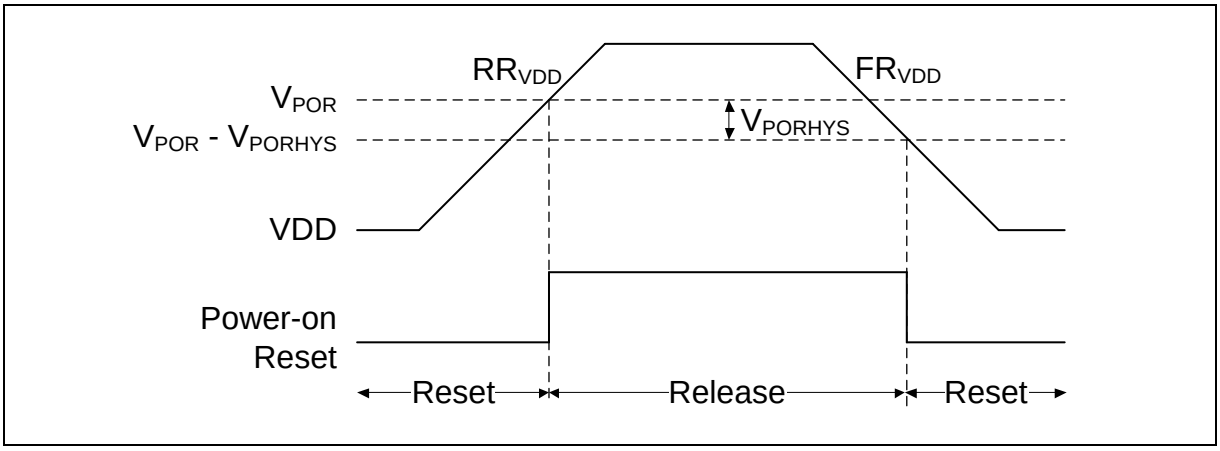


Figure 7.5-1 Power-on Reset Condition

7.6 USB Characteristics

7.6.1 USB Full-Speed Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input High (driven)	2.0	-	-	V	-
V_{IL}	Input Low	-	-	0.8	V	-
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended Receiver Threshold	0.8	-	2.0	V	-
	Receiver Hysteresis	-	200	-	mV	-
V_{OL}	Output Low (driven)	0	-	0.3	V	-
V_{OH}	Output High (driven)	2.8	-	3.6	V	-
V_{CRS}	Output Signal Cross Voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up Resistor		1.2		kΩ	-
Z_{DRV}	Driver Output Resistance	-	10	-	Ω	Steady state drive*
C_{IN}	Transceiver Capacitance	-	-	20	pF	Pin to GND

*Driver output resistance doesn't include series resistor resistance.

Table 7.6.1-1 USB Full-Speed Characteristics

7.6.2 USB Full-Speed PHY Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{FR}	Rise Time	4	-	20	ns	C_L=50p
T_{FF}	Fall Time	4	-	20	ns	C_L=50p
T_{FRFF}	Rise and Fall Time Matching	90	-	111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

Table 7.6.2-1 USB Full-Speed PHY Characteristics

7.6.3 USB VBUS Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{BUS}	VBUS Pin Input Voltage		5.0		V	-

Table 7.6.3-1 USB VBUS Characteristics

7.7 VAD Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{VADIDLE}$	Operation Current Idle mode with VAD	-	1.25	-	mA	VDDA = VDD = 3.3 V HCLK = 3.072MHz (HIRC/16) DMIC_MCLK = 1.536 MHz (HIRC/32) DMIC_CLK = 384 kHz (DMIC_MCLK/4) Sample Rate = 8 kHz (Down sample 48) No load

Table 7.7-1 VAD Characteristics

Note: This table is guaranteed by characteristics result, not tested in production.

7.8 Flash DC Electrical Characteristic

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply Voltage	1.08	-	1.32	V	T_A = 25 ℃
N_{ENDUR}	Endurance	10000	-	-	cycles[2]	
T_{RET}	Data Retention	10	-	-	year	
T_{ERASE}	Page Erase Time	92	-	160	ms	
T_{MER}	Mass Erase Time	300	-	350	ms	
T_{PROG}	Program Time	42	-	50	us	
I_{DD1}	Read Current	-	-	4.12	mA	
I_{DD2}	Program Current	-	-	5	mA	
I_{DD3}	Erase Current	-	-	5	uA	

Notes:

1. VFLA is source from chip LDO output voltage.
2. Number of program/erase cycles.
3. This table is guaranteed by design, not test in production.

Table 7.8-1 Flash DC Electrical Characteristics

7.9 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 7.9-1 I²C Dynamic Characteristics

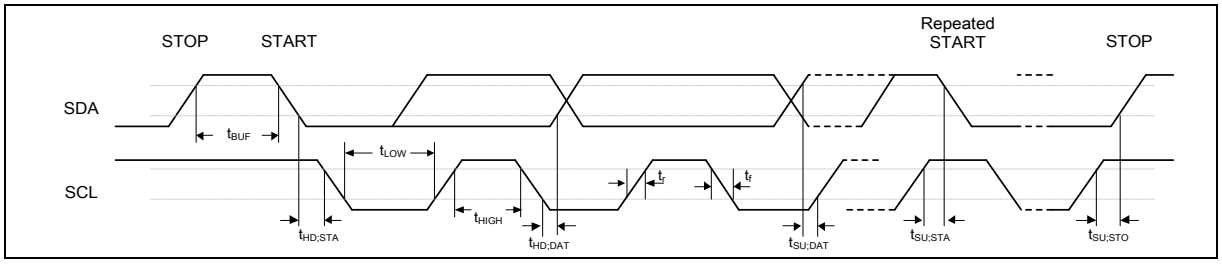


Figure 7.9-1 I²C Timing Diagram

7.10 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (VDD = 1.8 V~3.6V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20 MHz	22.5	-	27.5	ns
t_{DS}	Data input setup time	2	-	-	ns
$t_{H(MI)}$	Data input hold time	4	-	-	ns
t_V	Data output valid time	-	-	1	ns
$t_{H(MO)}$	Data output hold time	0	-	-	ns
SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20 MHz	22.5	-	27.5	ns
t_{DS}	Data input setup time	2			ns
$t_{H(MI)}$	Data input hold time	4			ns
t_V	Data output valid time		-	1	ns
$t_{H(MO)}$	Data output hold time	0	-	-	ns

Table 7.6.3-1 Dynamic Characteristics of Data Input and Output Pin in Master Mode

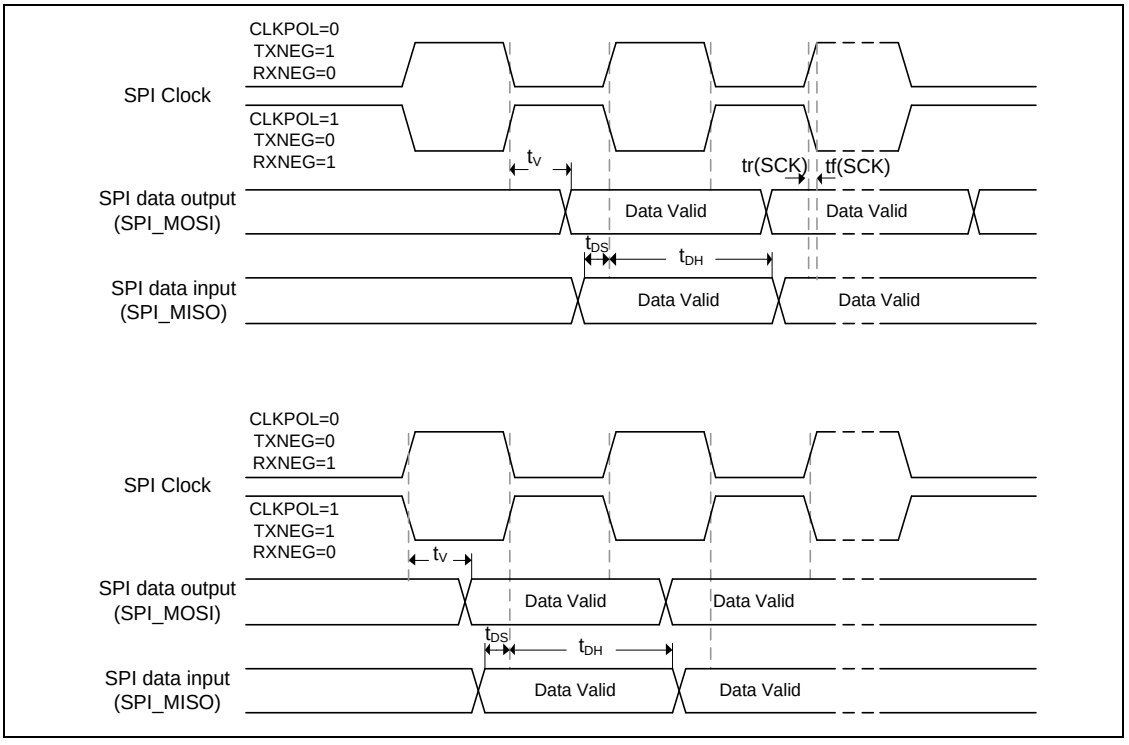


Figure 7.10-1 SPI Master Mode Timing Diagram

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI SLAVE MODE (VDD = 1.8 V~3.6V, 30 PF LOADING CAPACITOR)					
t_{SS}	Slave select setup time	3	-	-	Peripheral clock
t_{SH}	Slave select hold time	2	-	-	Peripheral clock
t_{DS}	Data input setup time	2	-	-	ns
$t_{H(SI)}$	Data input hold time	5.5	-	-	ns
$t_{a(SO)}$	Data output access time	-	-	18	ns
t_V	Data output valid time	-	18.5-	24.5	ns
$t_{H(SO)}$	Data output hold time	6	-	-	ns
SPI SLAVE MODE (VDD = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)					
t_{SS}	Slave select setup time	3	-	-	Peripheral clock
t_{SH}	Slave select hold time	2	-	-	Peripheral clock
t_{DS}	Data input setup time	2	-	-	ns
$t_{H(SI)}$	Data input hold time	6	-	-	ns
$t_{a(SO)}$	Data output access time	-	-	24	ns
t_V	Data output valid time	-	23	30	ns
$t_{H(SO)}$	Data output hold time	7	-	-	ns

Table 7.6.3-2 Dynamic Characteristics of Data Input and Output Pin in Slave Mode

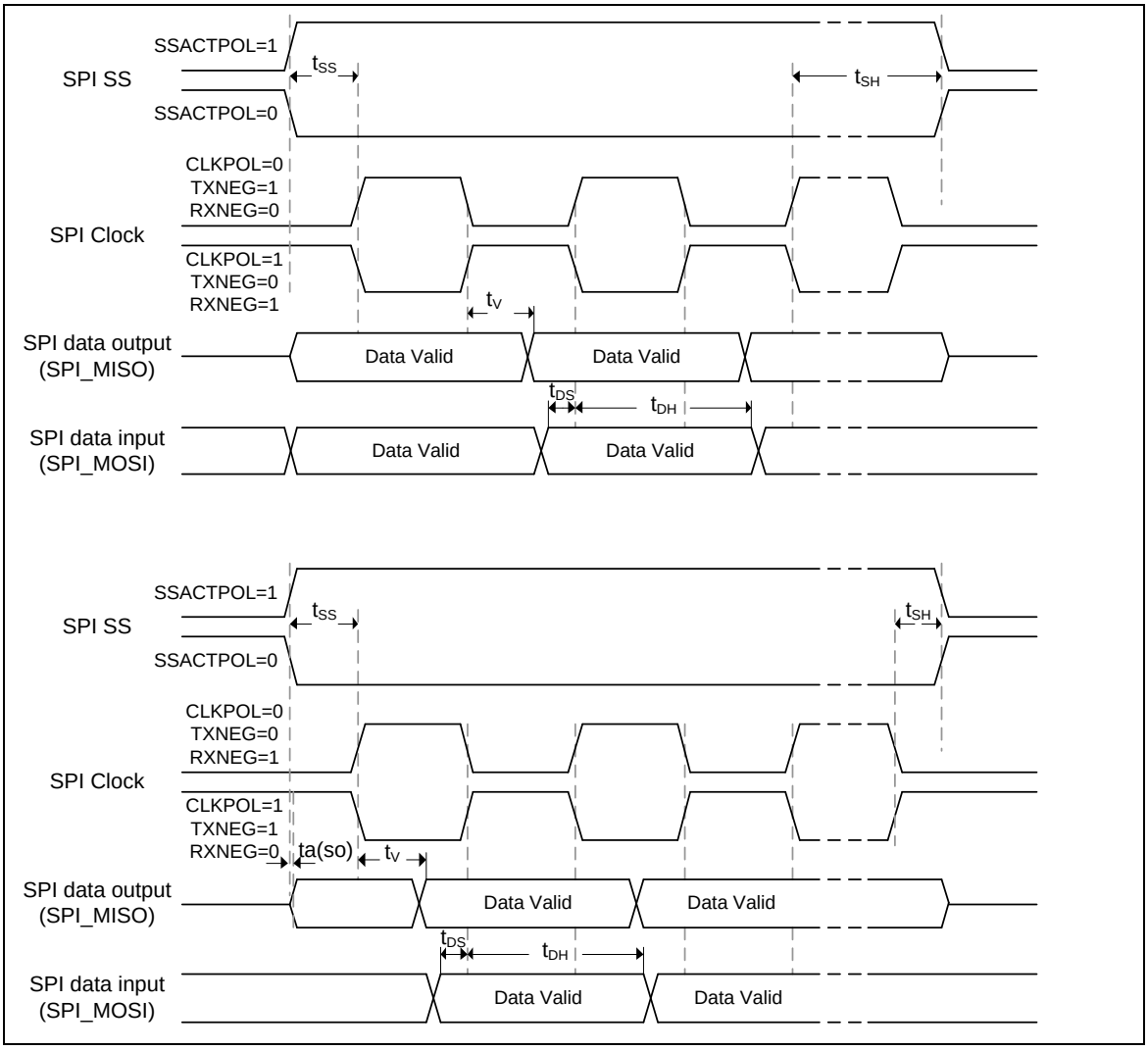


Figure 7.10-2 SPI Slave Mode Timing Diagram

7.11 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	-		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Table 7.11-1 I²S Dynamic Characteristics

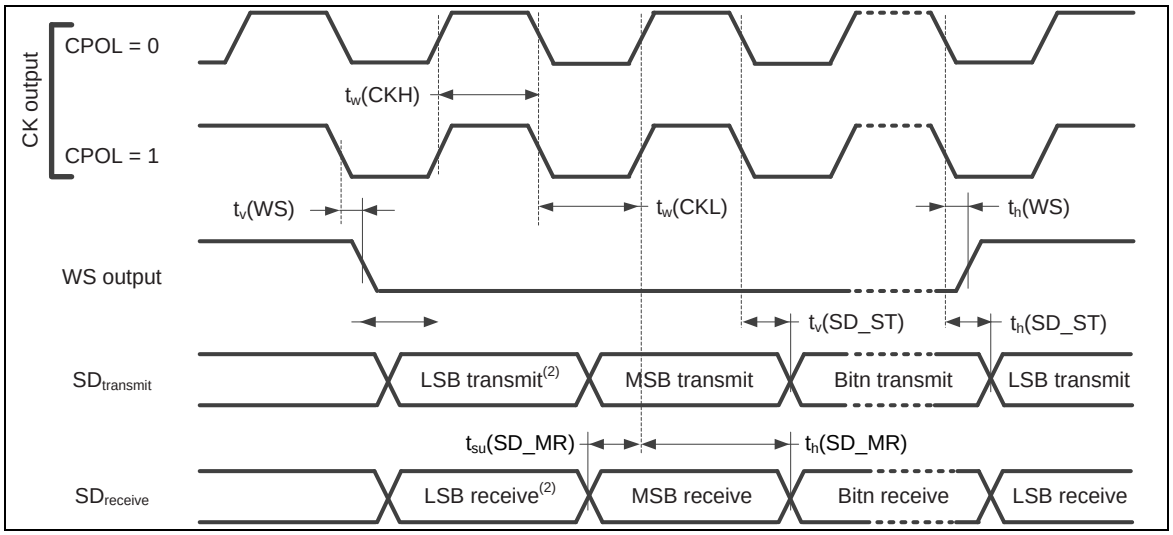


Figure 7.11-1 I²S Master Mode Timing Diagram

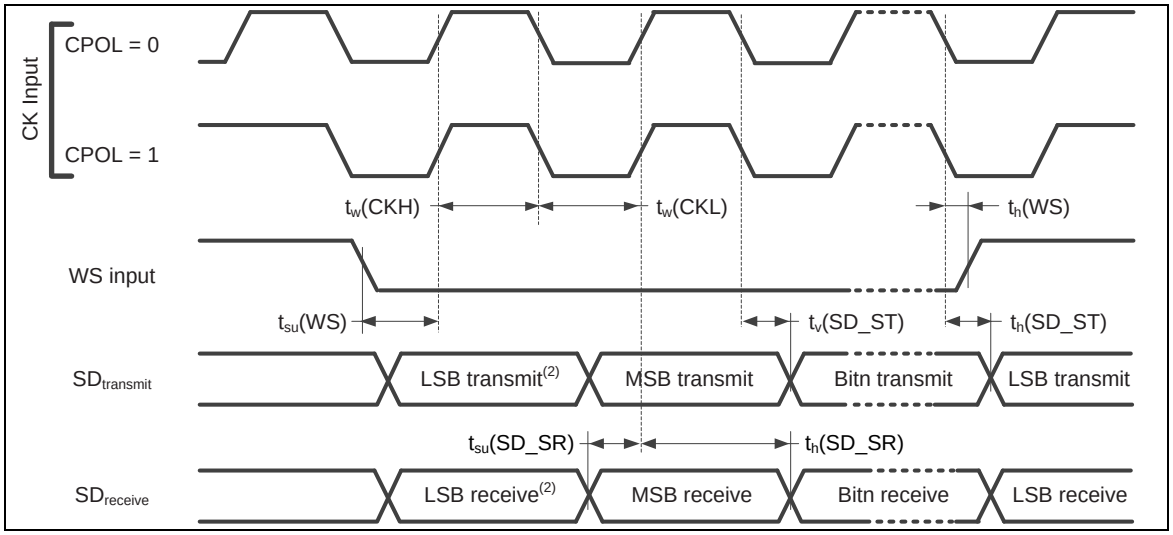


Figure 7.11-2 I²S Slave Mode Timing Diagram

8 APPLICATION CIRCUIT

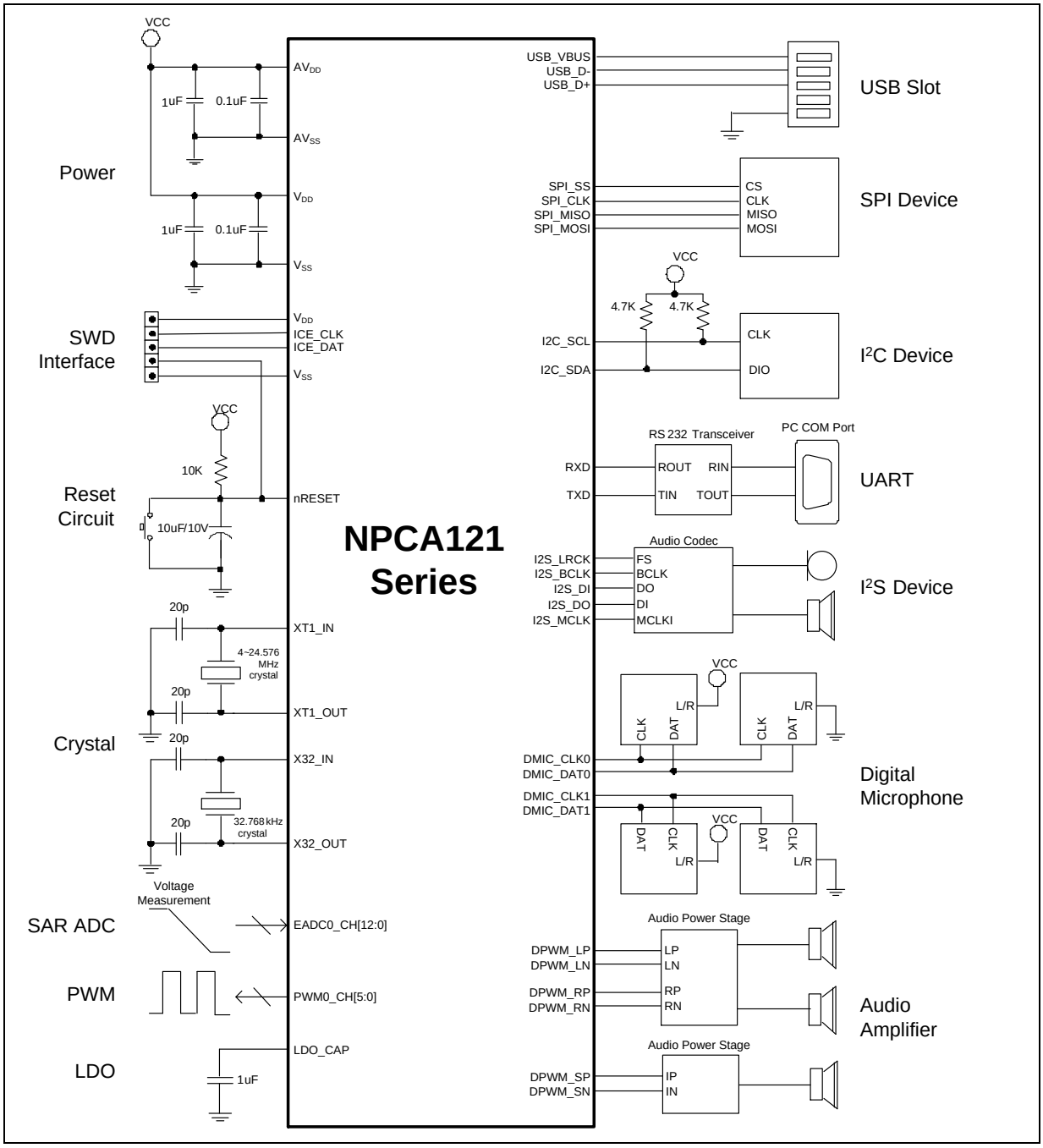
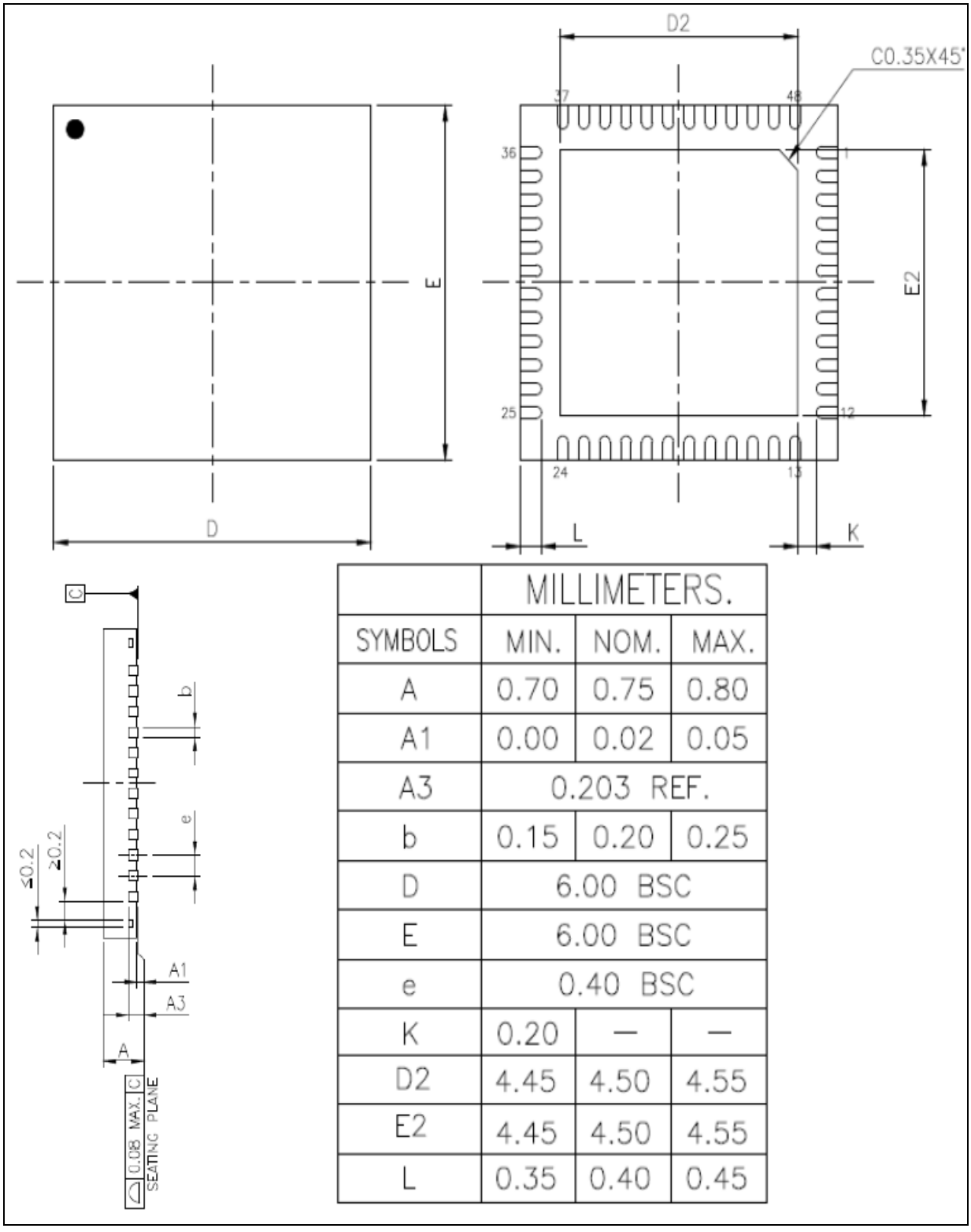


Figure 8-1 Application Circuit

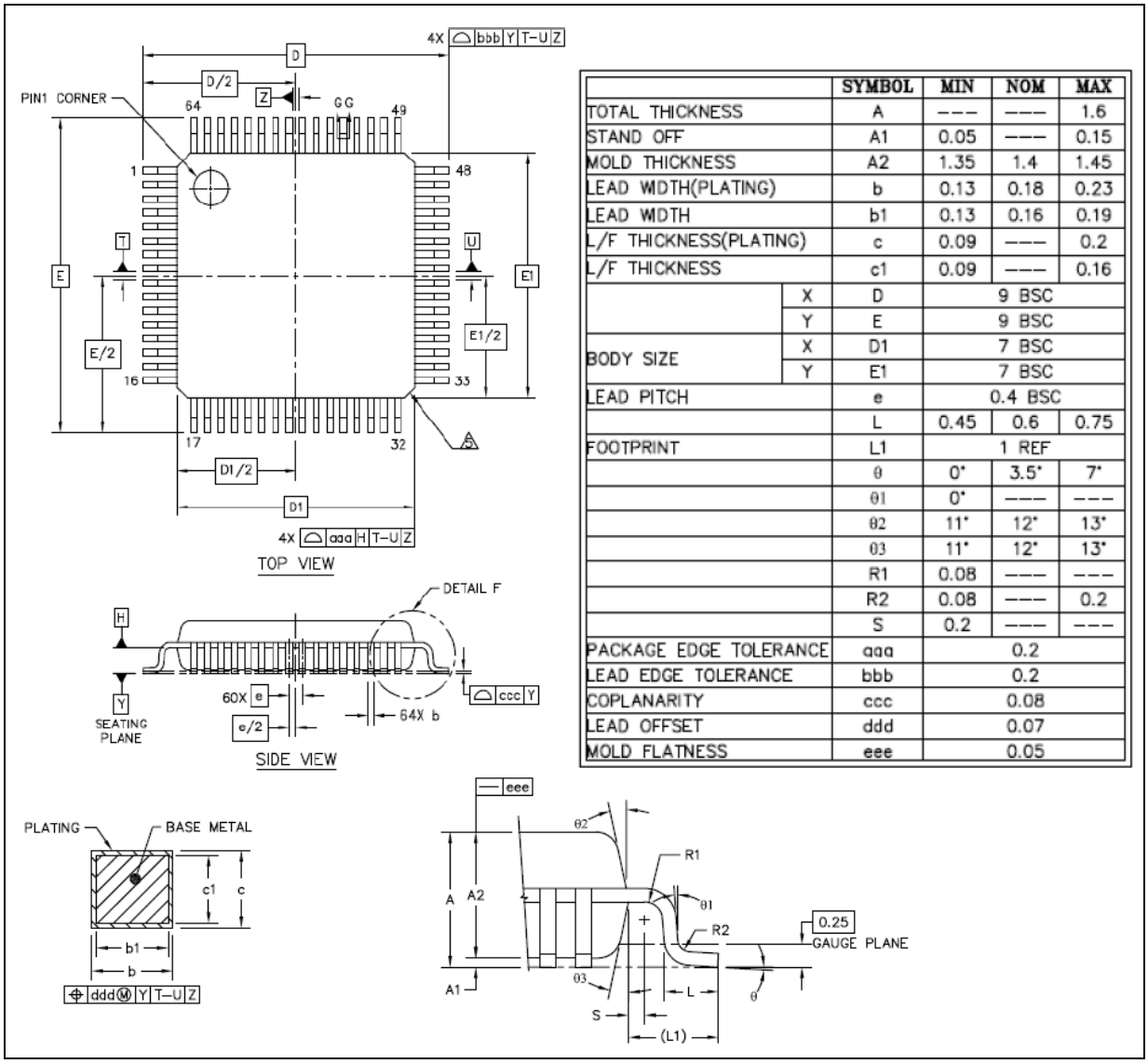
9 PACKAGE DIMENSIONS

9.1 QFN 48L (6x6x0.8 mm^3 Pitch 0.4 mm)



	MILLIMETERS.		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
e		0.40 BSC	
K	0.20	—	—
D2	4.45	4.50	4.55
E2	4.45	4.50	4.55
L	0.35	0.40	0.45

9.2 LQFP 64L (7x7x1.4 mm³ footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

10 REVISION HISTORY

Date	Revision	Description
2019.10.28	0.1	1. Preliminary version release

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