NPCA120
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The Nuvoton NPCA120 is a member of Nuvoton's Sound Enhancing family optimized for portable devices such as docking stations for Mobile phone, Multi-Media speakers, PC monitor speakers and Boom boxes.

The NPCA120 integrates Bongiovi sound enhancement algorithms. These are proprietary, patented, psychoacoustic algorithms that compensate for the acoustic limitations of small CE devices. The Bongiovi algorithms enable reproduction of rich content, with a wide dynamic range and a full frequency range, on a limited audio system.

The NPCA120 is also equipped with a variety of peripheral devices, such as I^2C, I^2S, USB, Low voltage reset and Brown-out Detector.

The NPCA120 is suitable for a wide range of applications such as:

- T.V. Speaker
- Monitor Speaker
- Boombox
- Soundbar
- Multi-Media Speker
- Docking Station

2 FEATURES

2.1 Peripherals

- I²S
  - Supports two I²S interface
  - Interface with external audio CODEC
  - Supports Master and Slave mode
  - Support two sample rate, 48KHz or 44.1KHz, with external crystal.
  - Capable of handling 16-bit, 24-bit and 32-bit word sizes
  - Mono and stereo audio data
  - I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
  - PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- USB
  - Compliant with USB 2.0 Full-Speed specification
  - Supports Isochronous transfer
  - Supports power saving mode when system enter suspend
- I²C
  - Supports Slave mode with 4 address selection.
  - Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Clock
  - External high speed crystal oscillator for precise timing operation.
- Built-in LDO for wide operating voltage range

2.2 Audio Enhancement

- Bongiovi Algorithm Inside
- Bongiovi AGC
- Bongiovi Multi-Band DRC
- Bongiovi Limiter with look-ahead
- Bongiovi Dynamic Stereo Enhancement
- Bongiovi Virtual Bass

2.3 Power Supply & Temperature

- Operating Voltage: 1.62 to 3.6 V
- Operating Temperature: -40℃~85℃

2.4 Package

- LQFP 64-pin (7x7 mm)
- QFN 48-pin (6x6 mm) –in developing

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Ordering Information

PART NUMBER	FEATURE	PACKAGE
NPCA120DD01	Standard	LQFP64
NPCA120DY02	Standard	QFN48

Table 3.1-1 Ordering Information

3.2 Pin Configuration

3.2.1 LQFP64 (7x7 mm) Pin Diagram

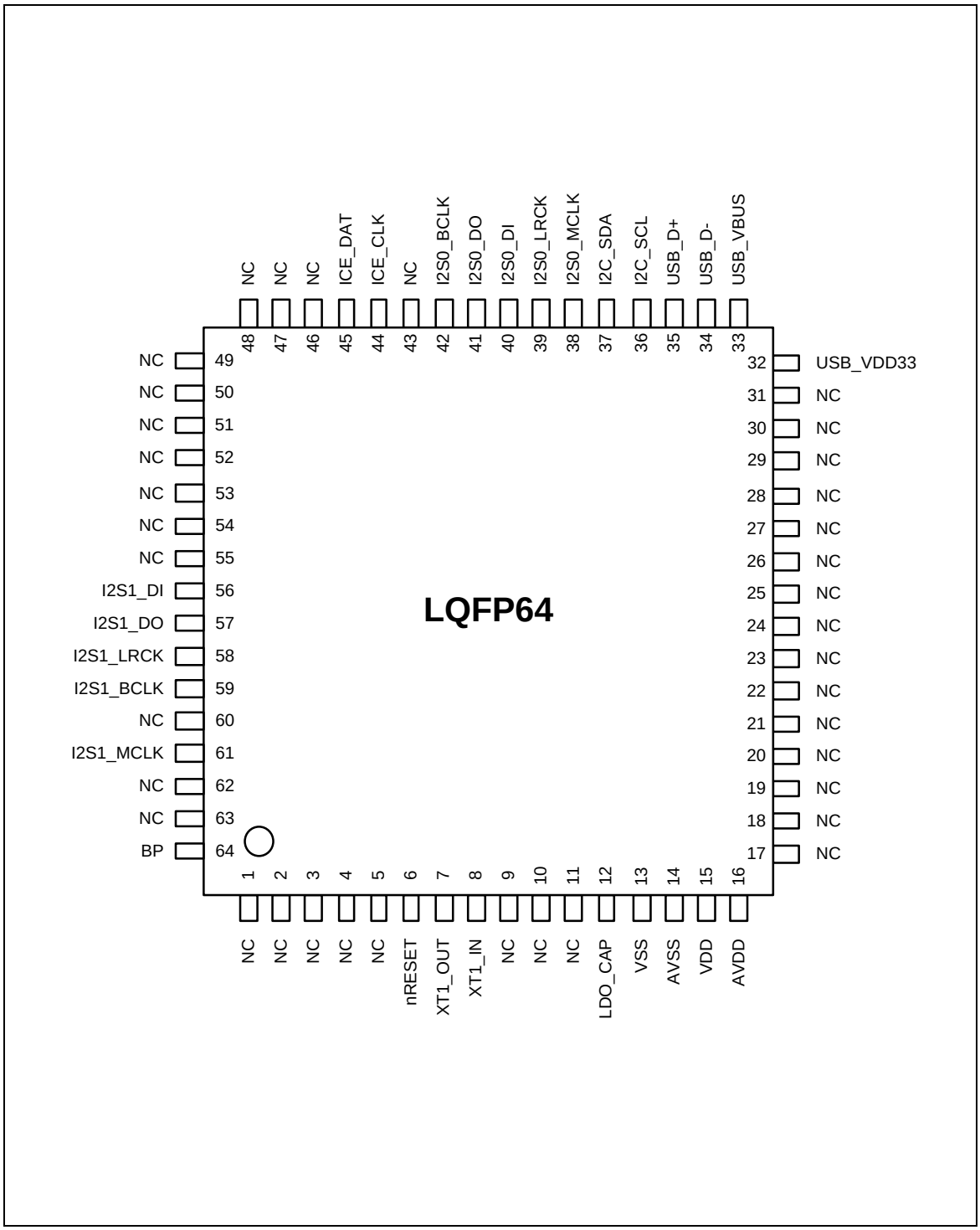


Figure 3.2-1 64-Pin LQFP64 Package

3.2.2 QFN48 (6x6 mm) Pin Diagram

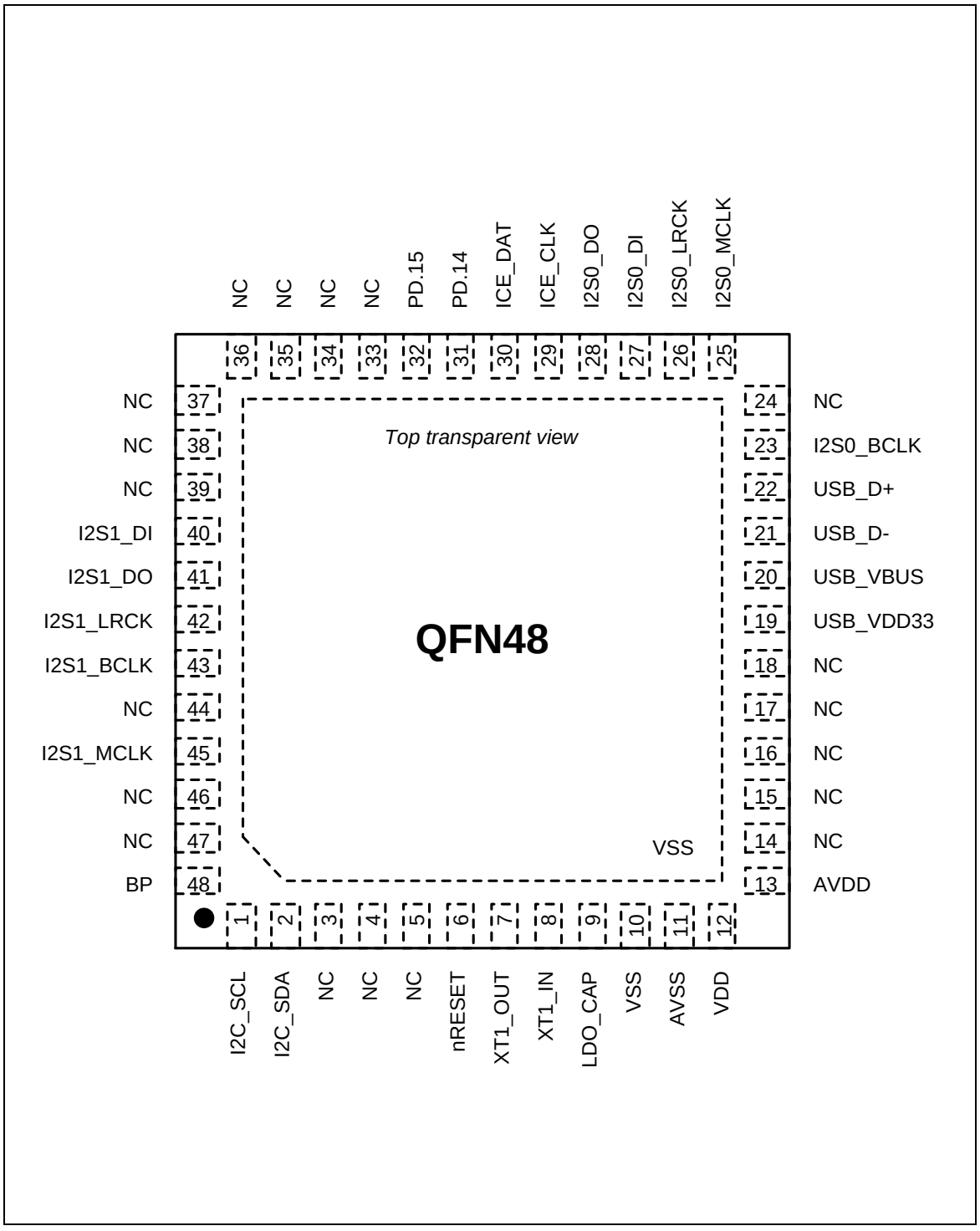


Figure 3.2-2 48-Pin QFN48 Package (In Developing)

3.3 Pin Description

Note: Pin Type I=Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

Pins		Pin Name	Type	Description
LQFP64 (7x7)	QFN48 (6x6)			
1		NC	-	No connection.
2	24	NC	-	No connection.
3	3	NC	-	No connection.
4	4	NC	-	No connection.
5	5	NC	-	No connection.
6	6	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
7	7	XT1_OUT	I	External 12.288 MHz (high speed) crystal output pin.
8	8	XT1_IN	I	External 12.288 MHz (high speed) crystal input pin.
9		NC	-	No connection.
10		NC	-	No connection.
11		NC	-	No connection.
12	9	LDO_CAP	P	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
13	10	VSS	P	Ground pin for digital circuit.
14	11	AVSS	P	Ground pin for analog circuit.
15	12	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
16	13	AVDD	P	Power supply for internal analog circuit.
17	14	NC	-	No connection.
18	15	NC	-	No connection.
19	16	NC	-	No connection.
20	17	NC	-	No connection.
21	18	NC	-	No connection.
22		NC	-	No connection.

Pins		Pin Name	Type	Description
LQFP64 (7x7)	QFN48 (6x6)			
23		NC	-	No connection.
24		NC	-	No connection.
25		NC	-	No connection.
26		NC	-	No connection.
27		NC	-	No connection.
28		NC	-	No connection.
29		NC	-	No connection.
30		NC	-	No connection.
31		NC	-	No connection.
32	19	USB_VDD33	P	Power supply for USB DC 3.3V
33	20	USB_VBUS	P	Power supply from USB or HUB.
34	21	USB_D-	A	USB differential signal D-.
35	22	USB_D+	A	USB differential signal D+.
36	1	I2C_SCL	I/O	I2C clock pin.
37	2	I2C_SDA	I/O	I2C data input/output pin.
38	25	I2S0_MCLK	O	I2S0 master clock output pin.
39	26	I2S0_LRCK	I/O	I2S0 left right channel clock pin.
40	27	I2S0_DI	I	I2S0 data input pin.
41	28	I2S0_DO	O	I2S0 data output pin.
42	23	I2S0_BCLK	I/O	I2S0 Bit Clock pin.
43		NC	-	No connection.
44	29	ICE_CLK	I	Serial wired debugger clock pin
45	30	ICE_DAT	I/O	Serial wired debugger data pin
46		NC	-	No connection.
47	31	NC	-	No connection.

Pins		Pin Name	Type	Description
LQFP64 (7x7)	QFN48 (6x6)			
48	32	NC	-	No connection.
49	33	NC	-	No connection.
50	34	NC	-	No connection.
51	35	NC	-	No connection.
52	36	NC	-	No connection.
53	37	NC	-	No connection.
54	38	NC	-	No connection.
55	39	NC	-	No connection.
56	40	I2S1_DI	I	I2S1 data input pin.
57	41	I2S1_DO	O	I2S1 data output pin.
58	42	I2S1_LRCK	I/O	I2S1 left right channel clock pin.
59	43	I2S1_BCLK	I/O	I2S1 Bit Clock pin.
60	44	NC	-	No connection.
61	45	I2S1_MCLK	O	I2S1 master clock output pin.
62	46	NC	-	No connection.
63	47	NC	-	No connection.
64	48	BP	-	Bypass algorithm. Note: This pin needs to be connected to VDD with a 10K resistor.

Table 3.3-1 Pin Description

4 BLOCK DIAGRAM

4.1 NPCA120 Block Diagram

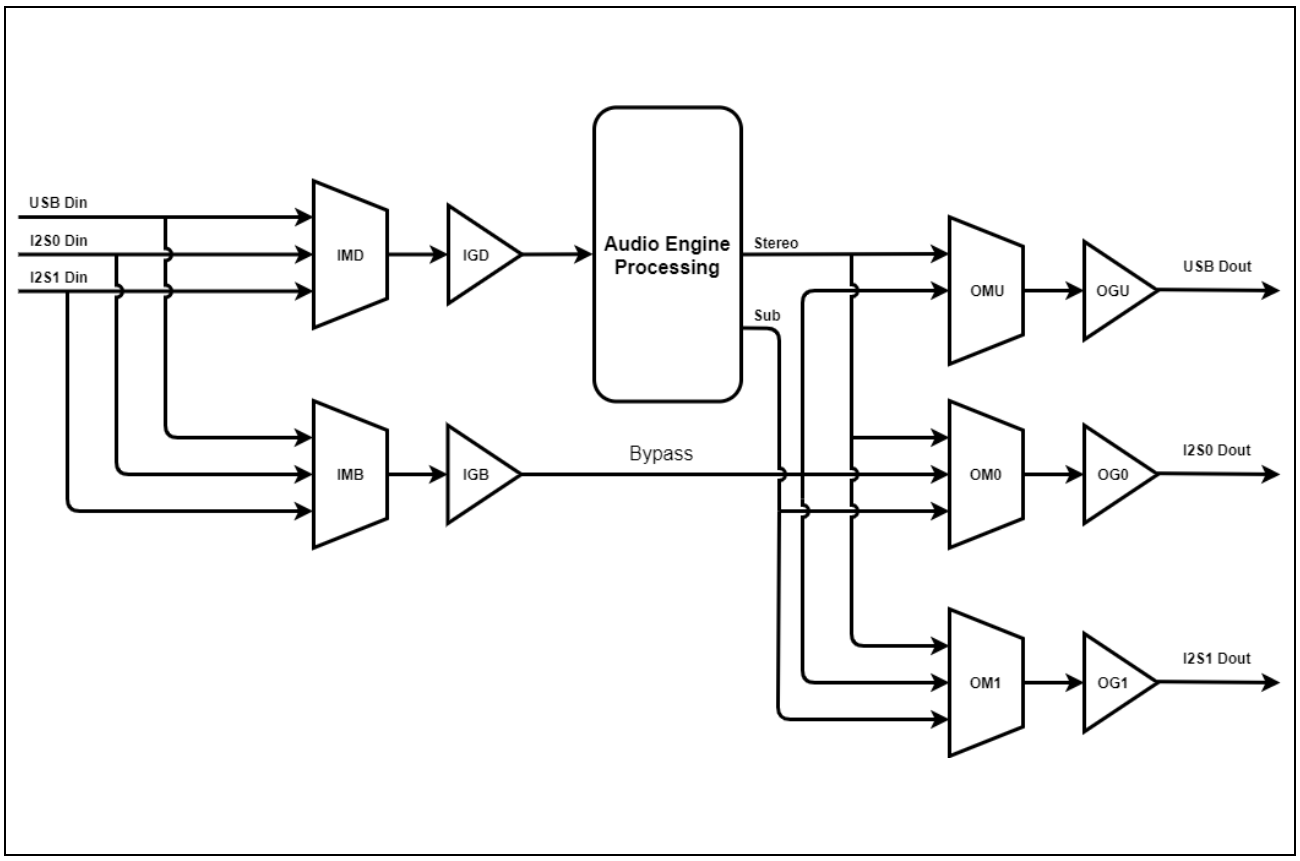


Figure 4.1-1 NPCA120 Block Diagram

5 FUNCTION DESCIPTION

5.1 Power

5.1.1 Power Distribution

NPCA120 power distribution is divided into:

- Analog power from AV_{DD} and AV_{SS} : provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} : supplies the power to the internal regulator which provides a regulated 1.2 V power for digital operation.
- USB transceiver power from USB_V_{DD33} offers the power for operating the USB transceiver.

Analog power (AV_{DD}) should be at the same voltage level as digital power (V_{DD}).

Both power supplies should have decoupling capacitors placed as close as possible to pins preferably with no via.

The outputs of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to LDO_CAP pin and returned directly to V_{SS}.

5.2 Clock

5.2.1 Overview

The clock diagram included processor and system clock, USB clock, I2S0 clock and I2S1 clock. The clock diagram also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The Figure 5.2-1 shows the clock diagram and the overview of the clock source control.

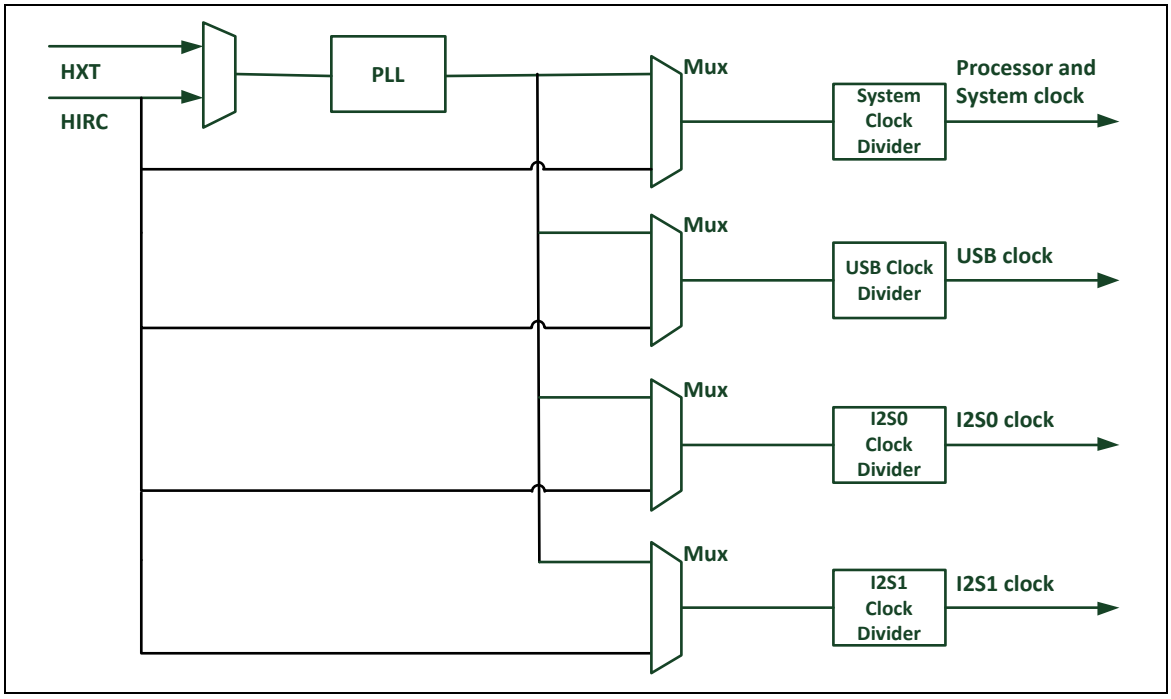


Figure 5.2-1 Clock diagram of NPCA120

5.2.2 Clock Source

Two clock sources can be used to drive all the internal clocks:

- 4~24.576 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24.576 MHz external high speed crystal (HXT) or internal high speed oscillator (HIRC)

5.3 I²S

5.3.1 Overview

The I²S bus consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively and is capable of handling 16/24/32 bits audio data sizes.

5.3.2 Features

- Support Master mode and Slave mode
- Capable of handling 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving

5.3.3 I²S Operation

The I²S bus supports different data format, I²S standard, I²S Left-Justified, I²S Right-Justified, PCM standard, PCM Left-Justified and PCM Right-Justified.

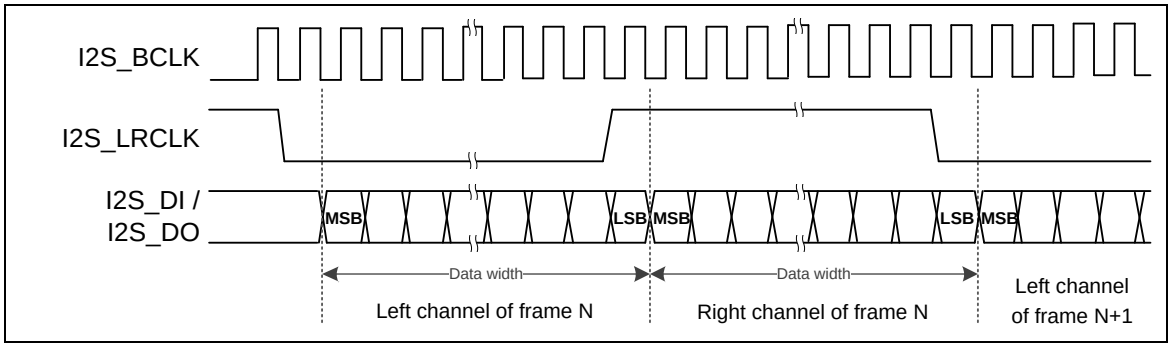


Figure 5.3-1 I²S Standard

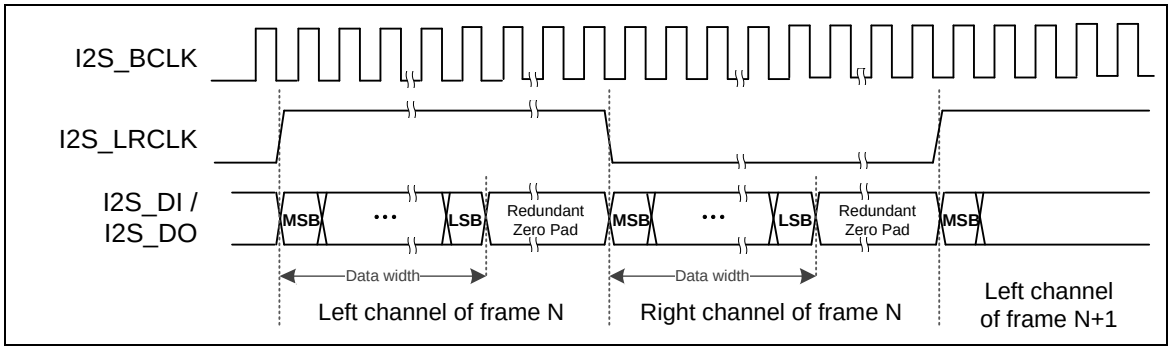


Figure 5.3-2 I²S Left-Justified

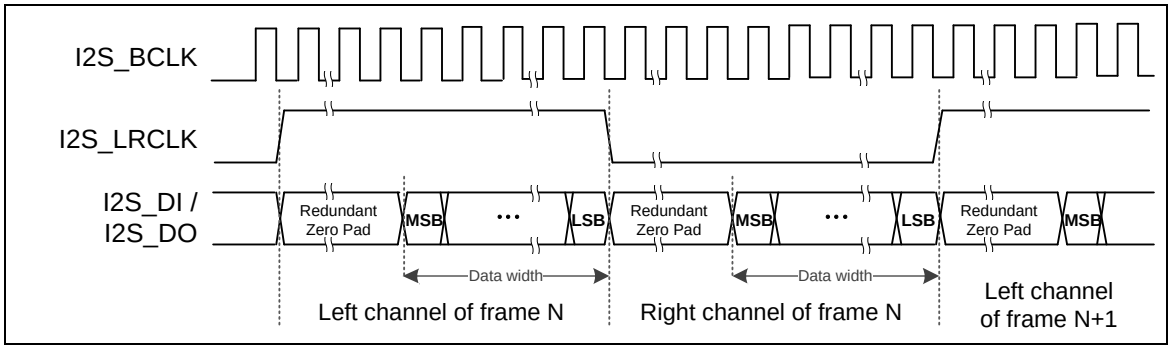


Figure 5.3-3 I²S Right-Justified

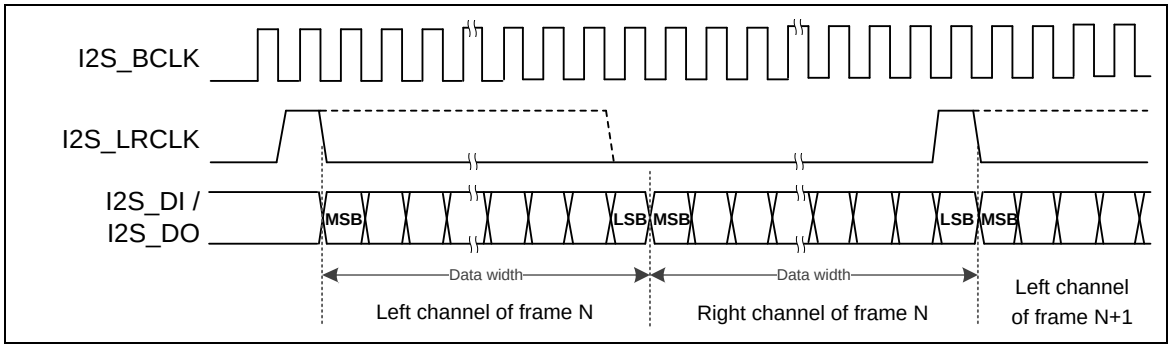


Figure 5.3-4 PCM Standard

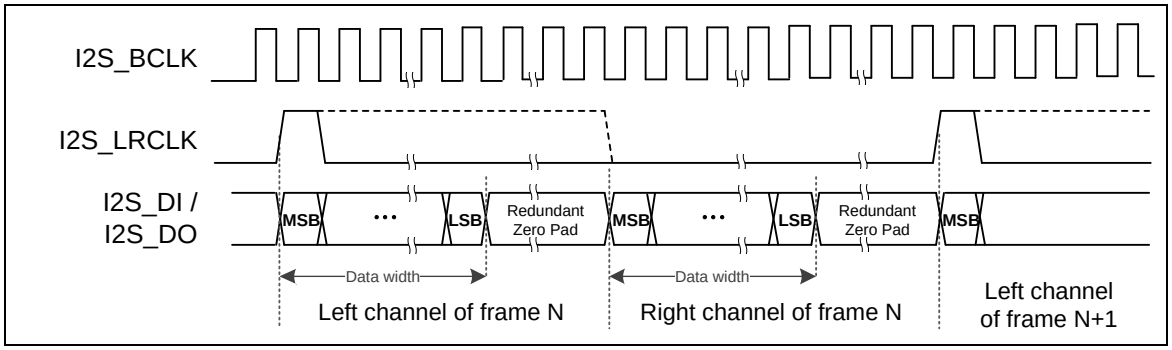


Figure 5.3-5 PCM Left-Justified

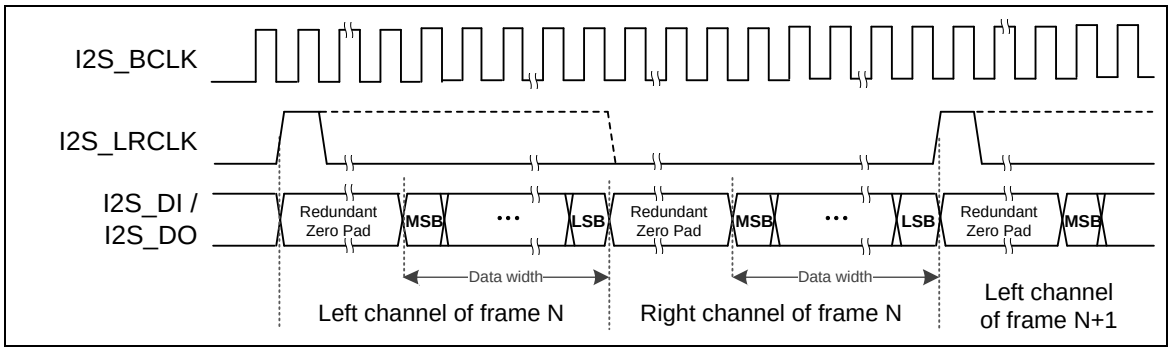


Figure 5.3-6 PCM Right-Justified

5.4 USB

5.4.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports isochronous transfer types.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

5.4.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Supports Isochronous transfer type
- Supports power saving mode when system enter suspend

5.5 I²C

5.5.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The NPCA120 device provides an I²C controller which can function as slave, support up to 1Mbs transfer rate.

5.5.2 Features

The NPCA120 I2C module supports the following features:

- Salve mode operation
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- 7-bit addressing mode
- Support four slave address for selection, 0x40 or 0x42 or 0x44 or 0x46.
- Power-down wake-up function

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

6.1.1 Voltage Characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+3.6	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
$\|V_{SS} – AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV

Note:

1. Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the life and reliability of the device.

Table 6.1.1-1 Voltage characteristics

6.1.2 Current Characteristics

Symbol	Parameter	Min	Max	Unit
– I_{DD}	Maximum Current into V_{DD}	-	200	mA
I_{SS}	Maximum Current out of V_{SS}	-	100	

Table 6.1.2-1 Current characteristics

6.1.3 Thermal Characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	

Table 6.1.3-1 Thermal characteristics

6.1.4 Electrostatic Discharge (ESD) Ratings

Symbol	Ratings	Max	Unit
V_{ESD}	ESD for Human Body Model (HBM)	4	kV

Note:

1. This is guaranteed by characterization results, not tested in production

Table 6.1.4-1 Electrostatic Discharge (ESD) Ratings

6.2 General Operating Conditions

(V_{DD} - V_{SS} = 1.8 ~ 3.3 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Typical Operation Voltage	1.8[1]	-	3.3[1]	V	
AV_{DD}	Analong Operation Voltage	V_{DD}			V	
USB_V_{DD33}	USB Operation Voltage	3.0	-	3.6	V	
V_{LDO}	LDO Output Voltage		1.2		V	
C_{LDO}	LDO Output Capacitance on LDO_CAP Pin	-	1	-	uF	

Note:

1. The limitation of V_{DD} operation voltage is 1.62V ~ 3.6V.

Table 6.2-1 General Operating Conditions

6.3 DC Electrical Characteristics

(VDD - VSS = 1.8 ~ 3.3 V, TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VILS	Negative going threshold (Schmitt input), nRESET	-0.3	-	0.3 VDD	V	
VIHS	Positive going threshold (Schmitt input), nRESET	0.7 VDD	-	VDD + 0.3	V	
RRST	Internal nRESET pin pull up resistor	-	50	-	kΩ	
VILS	Schmitt input high voltage		0.6* VDD	0.75* VDD	V	
VIHS	Schmitt input low voltage	0.3* VDD	0.4* VDD		V	

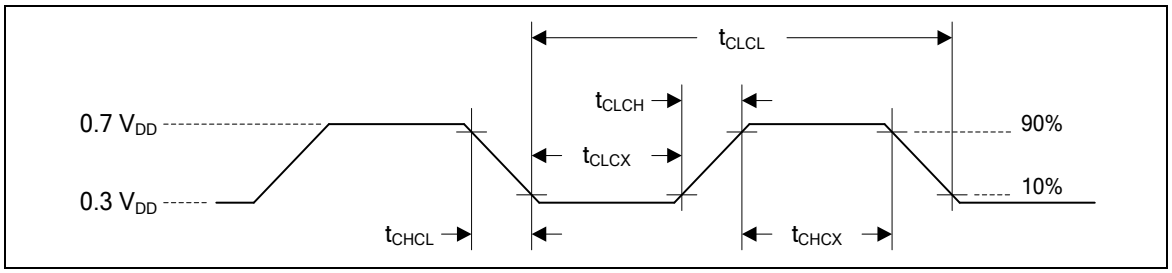
Notes:

1. nRESET pin is a Schmitt trigger input.

Table 6.3-1 DC Electrical Characteristics

6.4 AC Electrical Characteristics

6.4.1 External High Speed Crystal (HXT) Characteristics



Note:

1. Duty cycle is 50%.
2. Guaranteed by design, not tested in production

Figure 6.4.1-1 External High Speed Crystal Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

Table 6.4.1-1 External High Speed Clock Input Characteristics

6.4.1.1 HXT Typical Crystal Application Circuit

CRYSTAL	C_1	C_2
4 MHz ~ 24.576 MHz	Optional (depending on the crystal specification)	

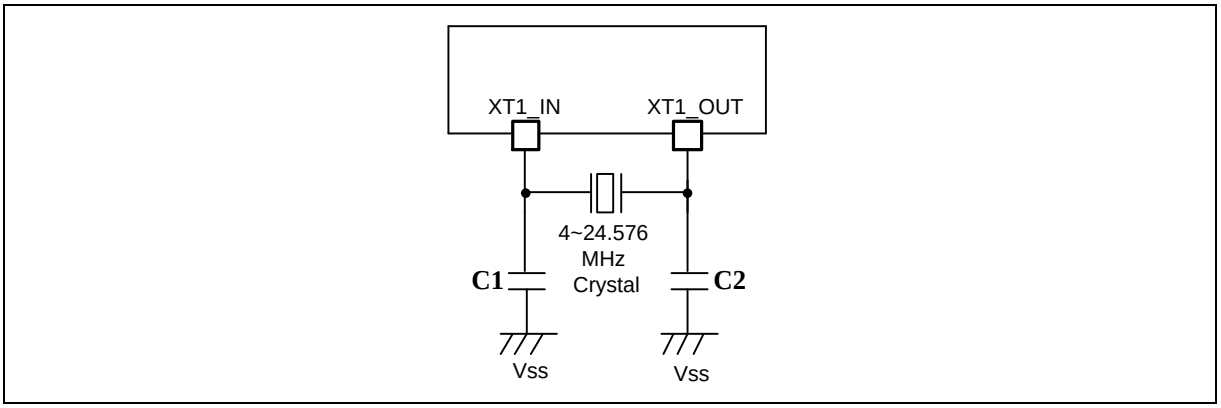


Figure 6.4.1-2 HXT Typical Crystal Application Circuit

6.4.2 Internal High Speed RC Oscillator (HIRC) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{HRC}	Operation Temperature	-40	25	85	℃	-
f_{HRC}	Center Frequency	-	49.152		MHz	-
	Calibrated Internal Oscillator Frequency	-	±0.25	-	%	T_A = 25 ℃ V_{DD} = 3.3 V
		-2	-	+2	%	T_A = -40℃~ 85 ℃
I_{HRC}	Operating Current	-	200	-	μA	T_A = 25 ℃,V_{DD} = 3.3 V

Table 6.4.2-1 Internal High Speed RC Oscillator (HIRC) Characteristics

6.5 Analog Characteristics

6.5.1 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Power-on Reset Voltage		1.45		V	-
V_{PORHYS}	Power-on Reset Hysteresis	-	110	-	mV	-
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	0.01	-	-	ms/V	-
FR_{VDD}	VDD Falling Rate to Ensure Power-on Reset	0.5	-	-	ms/V	-

Table 6.5.1-1 Power-on Reset Characteristics

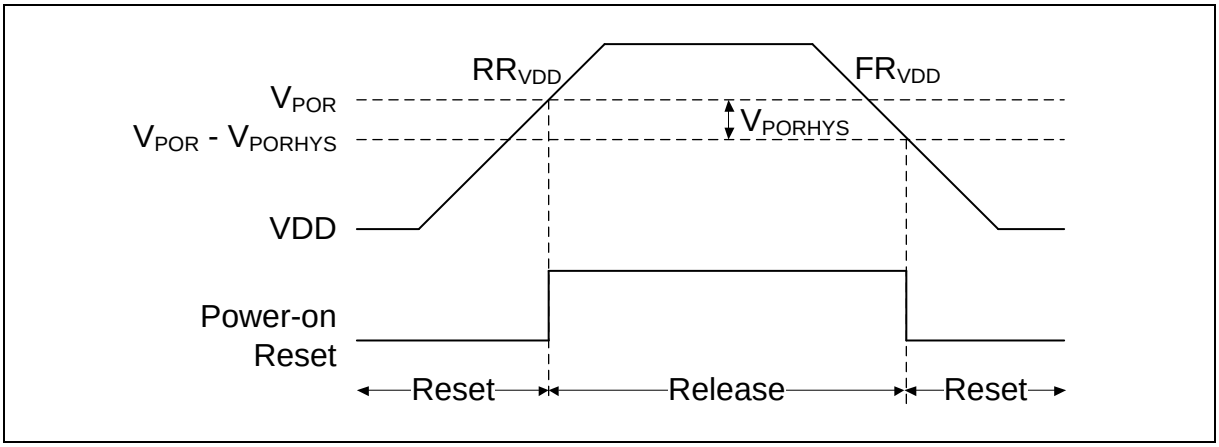


Figure 6.5-1 Power-on Reset Condition

6.6 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 6.6-1 I²C Dynamic Characteristics

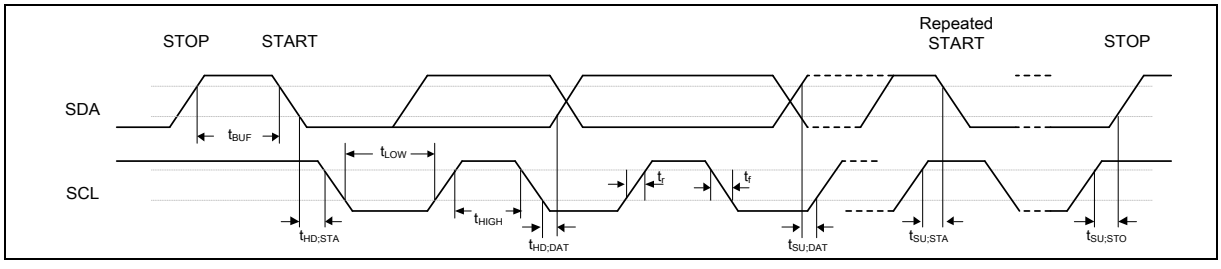


Figure 6.6-1 I²C Timing Diagram

6.7 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	-		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)
THD+N	Total Harmonic Distortion + Noise	0.0021	-	%	I2S0 bus, Master mode, Fs = 48K, word size = 16-bit
SNR	Signal to Noise Ratio		96	dB	

Table 6.7-1 I²S Dynamic Characteristics

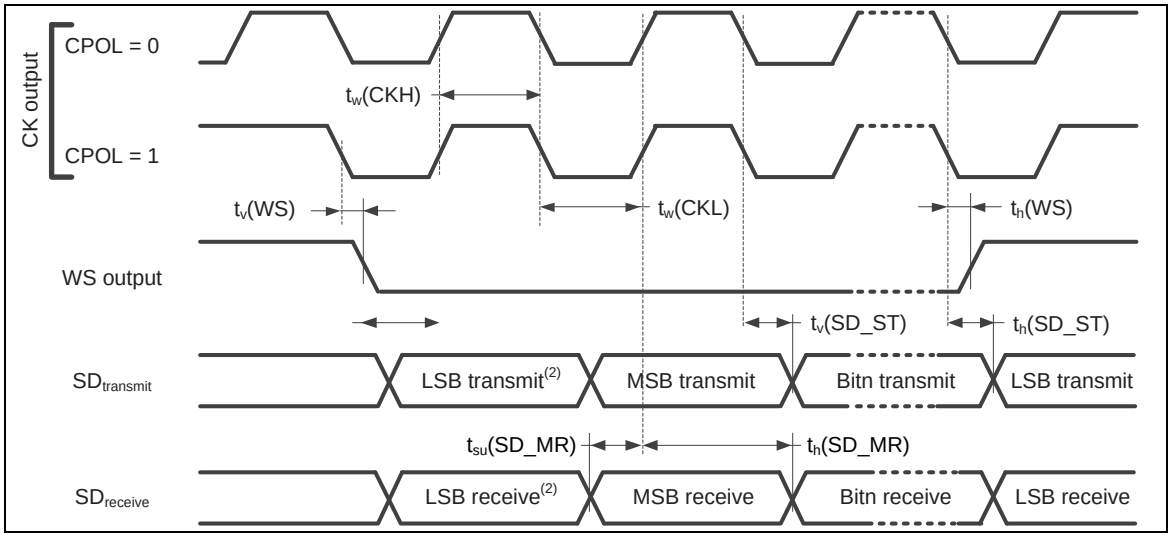


Figure 6.7-1 I²S Master Mode Timing Diagram

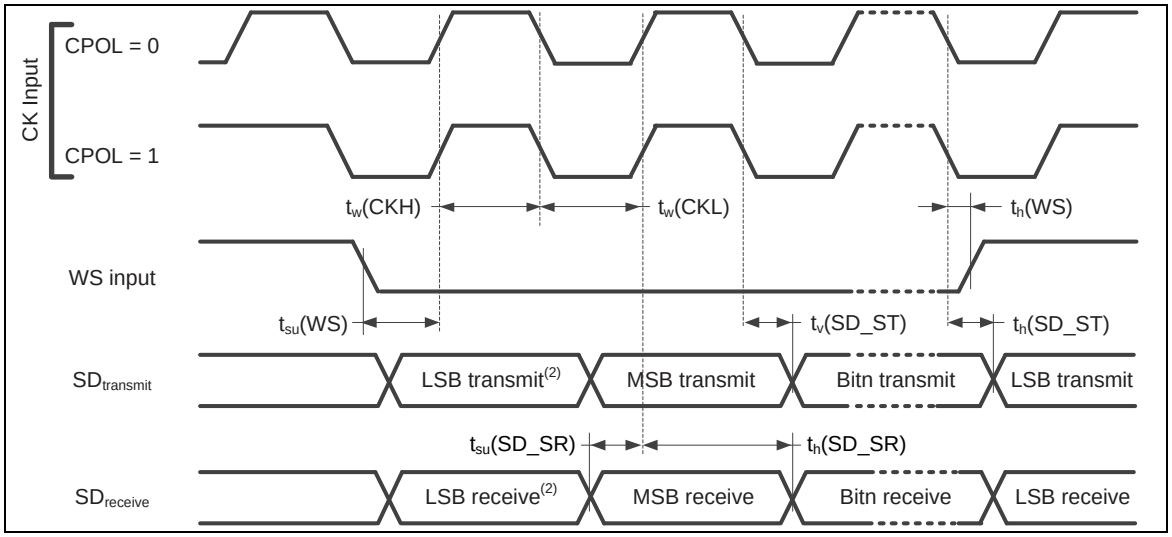


Figure 6.7-2 I²S Slave Mode Timing Diagram

7 APPLICATION CIRCUIT

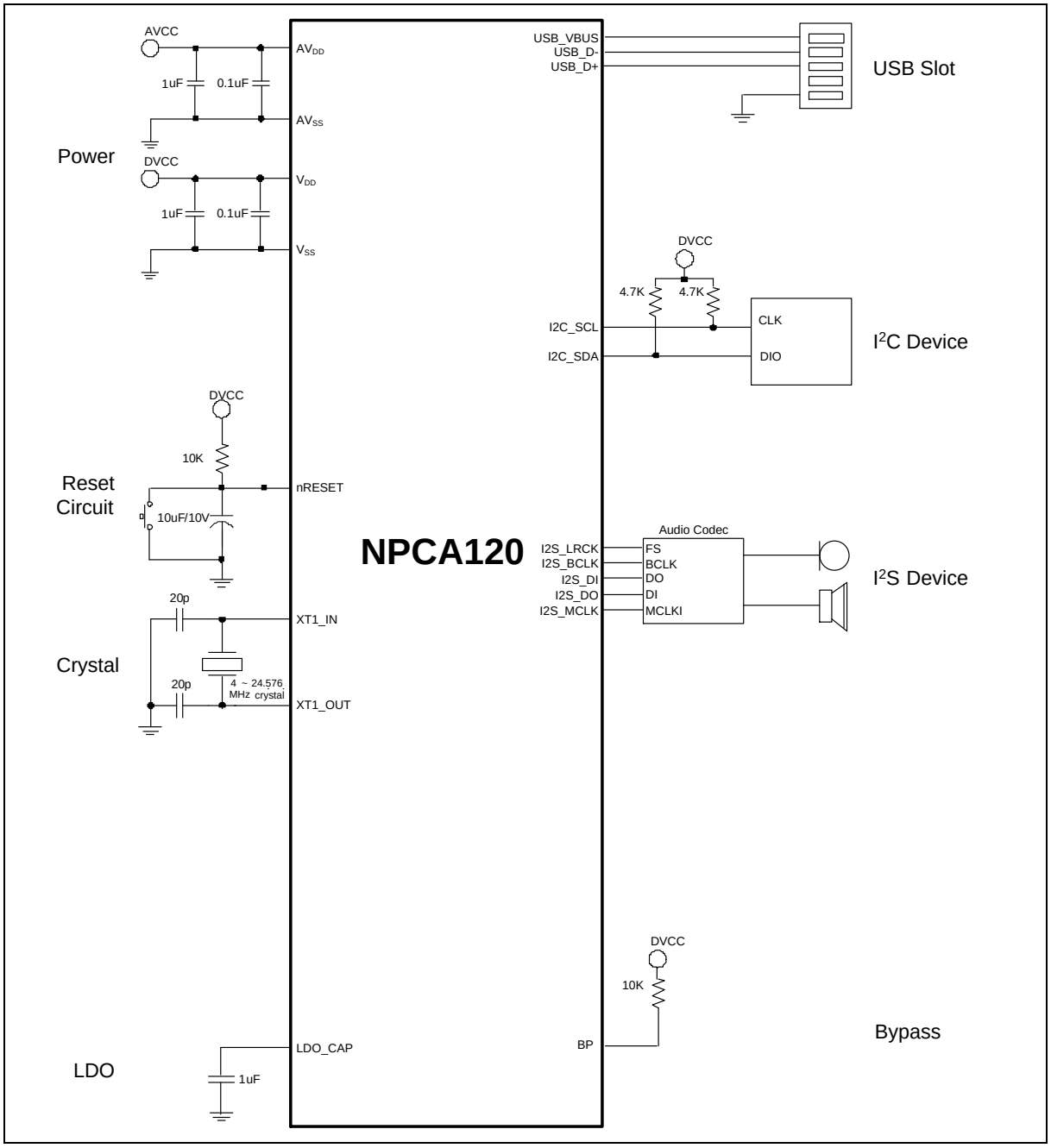
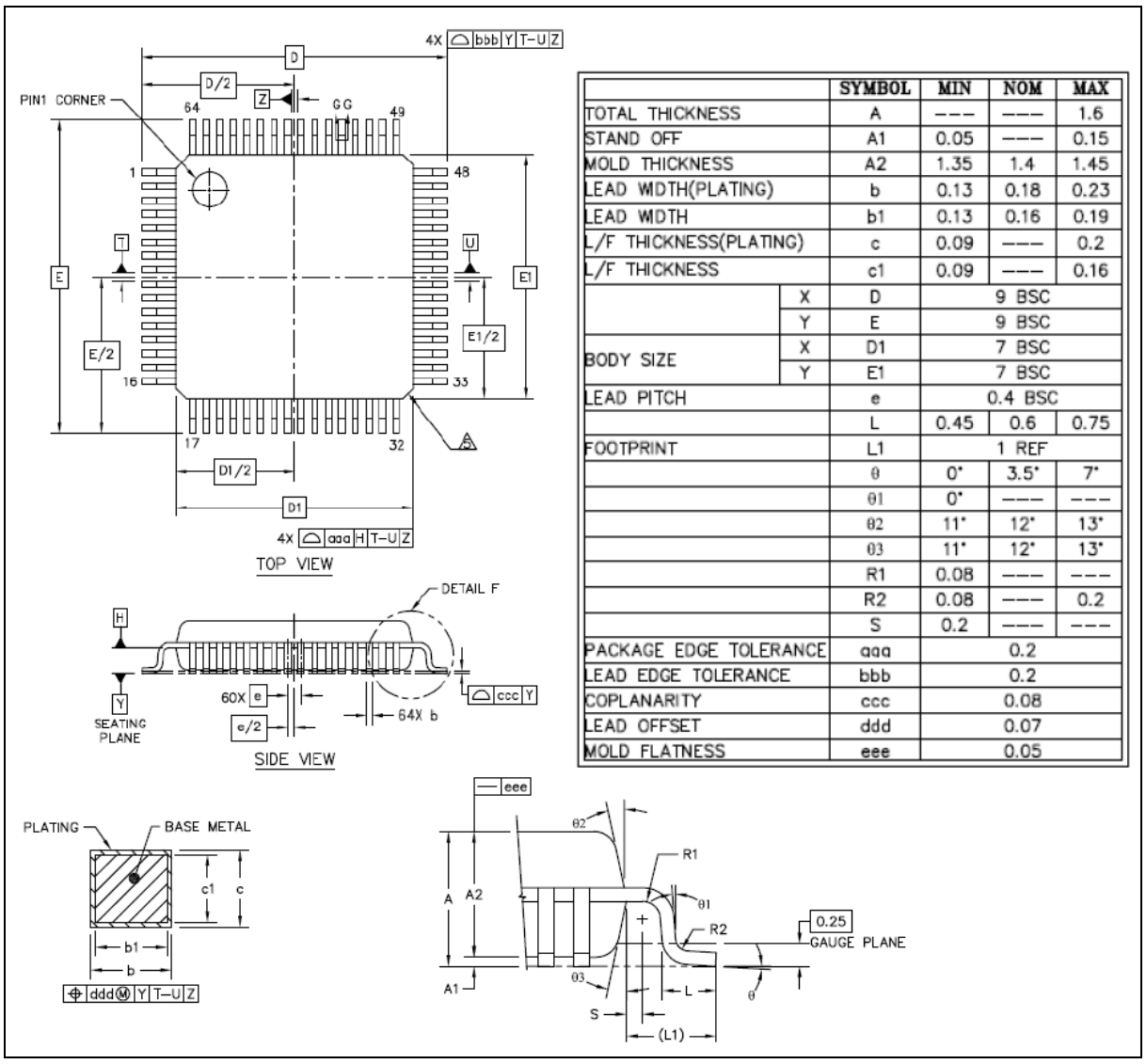


Figure 7-1 Application Circuit

8 PACKAGE DIMENSIONS

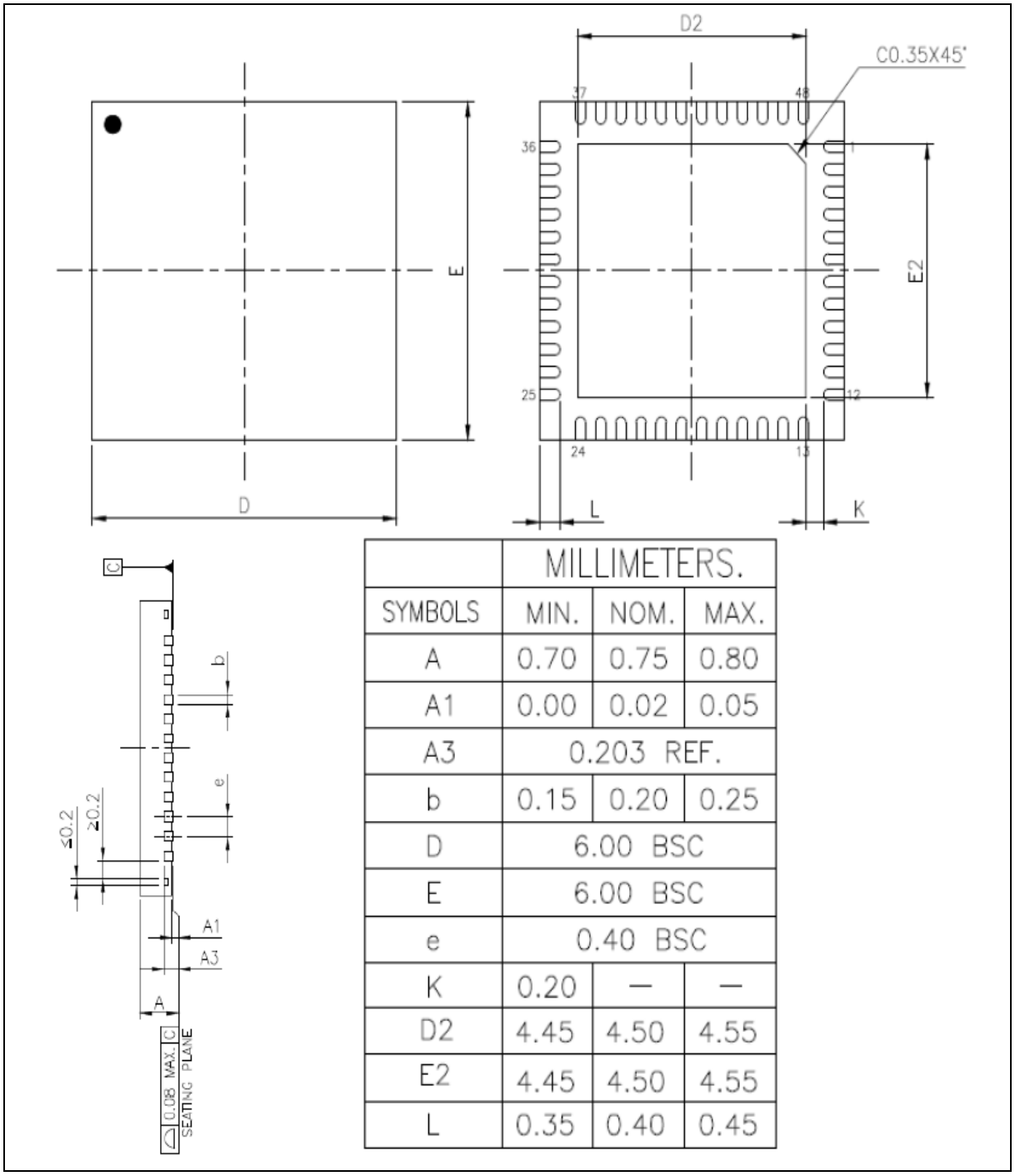
8.1 64-Pin LQFP (7x7x1.4 mm^3 footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

Figure 8.1-1 64-Pin LQFP Dimension

8.2 48-Pin QFN (6x6x0.8 mm³ Pitch 0.4 mm)



	MILLIMETERS.		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
e		0.40 BSC	
K	0.20	—	—
D2	4.45	4.50	4.55
E2	4.45	4.50	4.55
L	0.35	0.40	0.45

Figure 8.2-1 48-Pin QFN Dimension

9 REVISION HISTORY

Date	Revision	Description
2018.11.12	1.0	Brief version release
2019.03.29	1.1	Preliminary version release
2019.04.12	1.1	Modify typo
2019.11.04	1.12	Modify document
2019.11.20	1.13	Add QFN48 package, modify typo
2019.11.20	1.14	modify typo

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