ISD ARM® Cortex®-M4F SoC
ISD94100 Series
Datasheet

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1 GENERAL DESCRIPTION

The ISD94100 series 32-bit microcontrollers are an embedded ARM® Cortex®-M4F core with DSP extensions and a Floating Point Unit which run up to 200 MHz. It provides up to 512 KB of flash memory and up to 192 KB of SRAM. It is ideal for consumer product applications which need communication interfaces and high computing power.

The ISD94100 is also equipped with a variety of peripheral devices, such as Multi-Function Timers, Watchdog Timers, RTC, PDMA, UART, SPI, I^2C, PWM, GPIO, 12-bit ADC, USB1.1 Device, Low voltage reset and Brown-out Detector. In addition, it supports plenty of audio peripherals such as I^2S, DMIC and audio DPWM modulator.

The ISD94100 series is suitable for a wide range of applications such as:

- Audio Processing Platform
- Consumer Products
- Industrial Automation
- Home Automation
- Security Alarm System
- System Supervisors

2 FEATURES

2.1 Features

- Core
  - ARM® Cortex®-M4F core running up to 200 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Low Power Sleepmode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
  - Supports Embedded Trace Macrocell
- Built-in LDO for wide operating voltage range
- Flash Memory
  - Up to 512 KB on-chip Application ROM (APROM)
  - Configurable program code/data allocation
  - 4 KB on-chip Flash for user-defined loader (LDROM)
  - Supports 2-wire ICP update through SWD/ICE interface
  - Supports In-system program (ISP), In application program (IAP) update
  - Supports 4 KB page erase for all embedded flash
  - Supports 4 KB two-way cache to reduce power consumption and improve performance.
  - Enhanced performance up to 3.4 Core Mark/MHz when running code in Flash with cache
  - Supports 2-wire ICP flash updating through SWD interface
  - Supports 32-bit/64-bit and multi-word flash programming function.
  - Supports fast flash programming verification by CRC function.
- SRAM
  - Up to 192 KB embedded SRAM
  - 32 KB SRAM in bank 0 that supports hardware parity check and retention mode
  - Supports byte-, half-word- and word-access
  - Supports exception (NMI) generated once a parity check error occurs
  - Supports PDMA mode
- Clock Control
  - Built-in 48.0 MHz or 49.152 MHz selectable internal high speed RC oscillator (HIRC) for system operation.
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation.
  - 4~24.576 MHz external high speed crystal oscillator (HXT) for precise timing operation.
  - 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation.
  - Supports one PLL up to 500 MHz for high performance system operation, sourced from HIRC or HXT.
  - Supports clock failure detection for high/low speed external crystal oscillator.
  - Supports exception (NMI) generation once a clock failure detected.
  - Supports clock output.
- GPIO
  - Supports four I/O modes:
    - Quasi bi-direction

    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level trigger setting
  - Supports high slew driver and high sink current I/O (up to 20mA at 3.3V)
  - Supports software selectable slew rate control
  - Supports 5V tolerance function on subset of GPIO except analog I/O
- PDMA (Peripheral DMA)
  - Supports 16 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports stride function.
  - Channel 0, 1 supports time-out function for each channel.
  - Supports Basic and Scatter-Gather Transfer modes
  - Each channel supports circular buffer management using Scatter-Gather Transfer mode
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Supports single and burst transfer type
  - Supports source and destination address can be increment or fixed.
  - DMA transfer count up to 65536.
- Multi-Function Timer (MFT, Timer + PWM)
  - TIMER mode
    - Supports 4 sets of 32-bit timers with 24-bit up-timer and 8-bit prescale counter, 24-bit up counter value is readable.
    - Independent clock source for each timer
    - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
    - Supports event counting function to count the event from external pin
    - Supports input capture function to capture or reset counter value
    - Supports external capture pin event for interval measurement.
    - Supports external capture pin event to reset 24-bit up counter.
    - Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
    - Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC and DMA.
    - Supports Inter-Timer trigger mode
  - PWM mode
    - Supports four 16-bit PWM counters with 10-bit dead time generator
    - Supports 12-bit pre-scale for PWM.
    - Supports independent mode for PWM output channel
    - Supports 8 channel PWM outputs in complementary mode
    - Supports mask function and tri-state enable for each PWM pin
    - Supports interrupt on the following events:
      - PWM counter match zero, period value or compared value
    - Supports trigger EADC on the following events:
      - PWM counter match zero, period value or compared value
- PWM
  - Supports up to 6 independent PWM outputs with 16-bit resolution
  - Supports maximum clock frequency up to 200MHz
  - Supports 12-bit clock prescale
  - Supports dead time with maximum divided 12-bit prescale
  - Supports one-shot or auto-reload counter operation mode
  - Supports up, down or up-down PWM counter type
  - Supports synchronous function for phase control

- Supports counter synchronous start function
- Supports complementary mode for 3 complementary paired PWM output channel
- Supports brake function with auto recovery after brake condition removed
- Supports mask function and tri-state output for each PWM channel
- Supports trigger EADC to start conversion
- Supports up to 6 independent input capture channels with 16-bit resolution counter

- Watchdog Timer
  - 18-bit free running up counter for WDT time-out interval
  - Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
  - Configurable to force WDT enable after chip power-on or reset.
  - Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
- Window Watchdog Timer
  - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
  - Window set by 6-bit counter with 11-bit prescale
  - WWDT counter suspends in Idle/Power-down mode
- RTC
  - Supports software compensation by setting frequency compensate register (FCR),compensated clock accuracy reaches ±5ppm within 5 seconds
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports Day of the Week counter
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports 1 Hz, clock output
  - Supports wake-up from idle mode, Power-down mode and Standby Power-down mode
  - Supports 32 kHz Oscillator gain control
  - Supports RTC Time Tick and Alarm Match interrupt
  - Support Time stamp
- UART
  - Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped
  - Support baud rate up to 12.5 MHz
  - Supports 16-byte FIFOs with programmable level trigger
  - Supports auto flow control (CTS and RTS)
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Programmable receiver FIFO trigger level
  - Supports wake-up function
  - Supports 8-bit receiver FIFO time-out detection function
  - Supports Auto-Baud Rate measurement and baud rate compensation function
  - Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function
  - Supports nCTS, incoming data, RX FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode.
  - Supports hardware or software enables to program nRTS pin to control RS-485

transmission direction
- Supports PDMA mode

- I²C
  - Supports up to two sets of I²C devices
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Supports 10 bits mode
  - Support High speed mode 3.4Mbps
  - Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports SMBus and PMBus
  - Supports multi-address Power-down wake-up function
- I²S
  - Supports one I²S interface
  - Interface with external audio CODEC
  - Supports Master and Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Mono and stereo audio data
  - I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
  - PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
  - PCM protocol supports TDM multi-channel transmission in one audio sample, the number of data channels can be set as 2, 4, 6, or 8
  - Two 16-level FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- SPI0
  - SPI Quad controller – SPI0
  - Supports Master or Slave mode operation
  - Supports 2-bit Transfer mode
  - Supports Dual and Quad I/O Transfer mode
  - Supports one/two data channel half-duplex transfer
  - Support receive-only mode
  - Configurable bit length of a transfer word from 8 to 32-bit
  - Provides separate 8-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports the byte reorder function
  - Supports Byte or Word Suspend mode
  - Supports 3-wired, no slave select signal, bi-direction interface
  - Master up to 25 MHz, and Slave up to 25 MHz (when chip operating at V_{DD} = 2.7~3.6V)
  - Supports PDMA mode
- SPI / I²S
  - Supports two sets of SPI/ I2S controllers – SPI1/ SPI2
  - Supports Master or Slave mode operation

- Supports two PDMA requests, one for transmitting and the other for receiving
- SPI supports configurable bit length of a transfer word from 8 to 32-bit
- SPI Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
- SPI supports MSB first or LSB first transfer sequence
- SPI supports the byte reorder function
- SPI supports Byte or Word Suspend mode
- SPI supports one data channel half-duplex transfer
- SPI supports receive-only mode
- I2S interface with external audio CODEC
- I2S supports Master and Slave mode
- I2S supports 8-, 16-, 24- and 32-bit audio data sizes
- I2S supports mono and stereo audio data
- I2S supports PCM mode A, PCM mode B, I2S and MSB justified data format
- I2S Interface with external audio CODEC
- I2S provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary

- EADC
  - Analog input voltage range: 0~ AV_{DD}
  - Supports single 12-bit SAR EADC conversion
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Up to 13 external single-ended analog input channels
  - Up to 2 MSPS conversion rate
  - Supports three power saving modes:
    - Deep Power-down mode
    - Power-down mode.
    - Standby mode.
  - Supports single EADC interrupt
  - Supports calibration and load calibration words capability.
  - An A/D conversion can be triggered by Software enable, External pin, Timer 0~3 overflow pulse trigger and PWM trigger.
  - 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
  - Maximum EADC clock frequency is 60 MHz.
  - Configurable EADC internal sampling time.
  - Up to 13 sample modules
    - Each of sample module 0~12 which is configurable for EADC converter channel EADC_CH0~12 and trigger source.
    - Double buffer for sample module 0~3
    - Configurable sampling time for each sample module.
    - Conversion results are held in 13 data registers with valid and overrun indicators.
  - Supports PDMA transfer
- USB 1.1 Device Controller
  - Compliant with USB 2.0 Full-Speed specification
  - Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
  - Supports Control/Bulk/Interrupt/Isochronous transfer type
  - Supports suspend function when no bus activity existing for 3 ms
  - Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1k bytes buffer size
  - Provides remote wake-up capability
- Digital Microphone Inputs
  - Provides one 32-level FIFO data buffers for receiving.

- Generates interrupt requests when buffer levels cross a programmable boundary.
- Supports PDMA transfer.
- Supports up to four channel digital microphones.
- Both digital PDM microphone inputs can be used simultaneously.

- Voice Active Detection
  - Configuration detect levels.
  - Supports idle mode wake-up function.
  - Supports auto switch DMIC path when CPU wake-up by VAD.
  - Generates interrupt requests when voice detected.
- Audio DPWM Modulator
  - Differential Audio PWM Output (DPWM).
  - Supports left channel, right channel and sub-woofer channels.
  - Supports sample rates from 16~96 kHz.
  - Programmable biquad 10 band filter.
  - PDMA data channel for streaming of PCM audio data.
  - Supports either single precision floating point or fixed-point format input data and BIQ coefficients.
  - Provides 32-sample FIFO data buffer for PCM data.
- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports 8-/16-/32-bit of data width
  - Programmable seed value
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
  - Supports using DMA to write data to perform CRC operation
- Brown-out Detector
  - With 8 levels: 3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 1.5V
- Operating Temperature: -40℃~85℃
- Packages
  - All Green package (RoHS)
  - QFN 48-pin (6x6 mm)
  - LQFP 64-pin (7x7 mm)
  - LQFP 64-pin (10x10 mm)

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
DMIC	Digital Microphone Inputs
DPWM	Audio DPWM Modulator
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	High Speed RC Oscillator
HXT	External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
VAD	Voice Active Detection
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Parts Information

PART NUMBER		I941					
		24	24	13	24	23	13
Max. CPU frequency (MHz)		200					
Flash (KB)		512		256	512		256
SRAM (KB)		192		128	192	128	
ISP Loader ROM (KB)		4					
I/O		58	57		41		
32-bit Timer		4					
RTC		√					
PWM		6			5		
USB 1.1 FS Device		-	√				
12-bit ADC		13			12		
Connectivity	UART	1					
	SPI	1					
	SPI/I²S	2					
	I²S	1					
	I²C	2					
Audio Function	Audio DPWM	2.1					
	DMIC	4[1]	4				
	VAD	√					
Package		LQFP 64 (10x10 mm)	LQFP 64 (7x7 mm)		QFN 48 (6x6 mm)		

Table 4.1-1 Devices Features and Peripheral Counts

Note 1: Maximum CPU 100MHz when DMIC is used.

4.2 Ordering Information

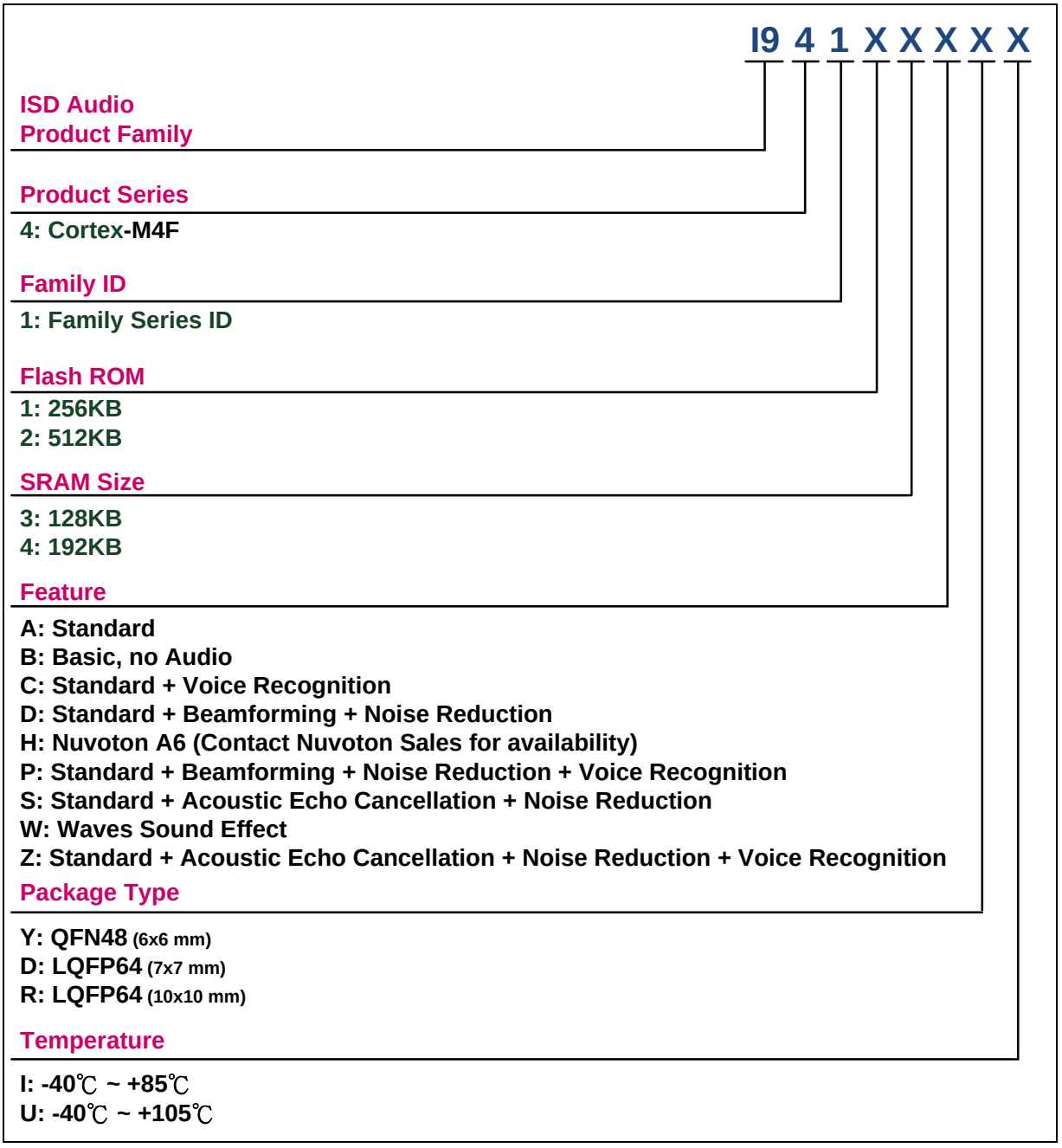


Figure 4.2-1 Ordering Information Scheme

Note:

1. The feature “B” do not provide DPWM and DMIC functionality.
2. The features “W” and “Z” are only available when the SRAM size is 192 KB and the flash memory size is 512 KB.

4.3 Pin Configuration

4.3.1 QFN48 (6x6 mm) Pin Diagram

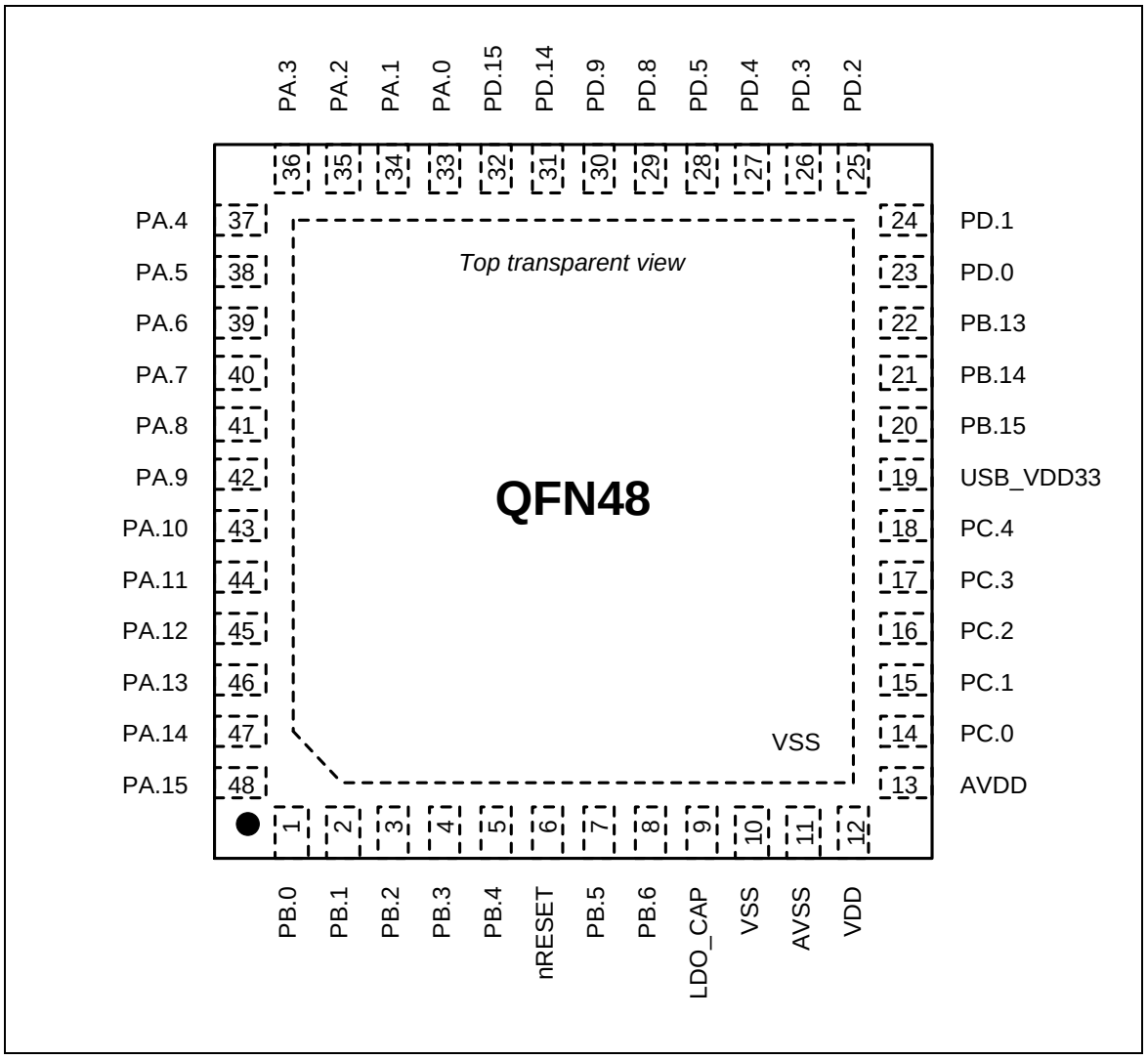


Figure 4.3-1 QFN48 (6x6 mm) Pin Diagram

4.3.2 LQFP64 (7x7 mm) Pin Diagram

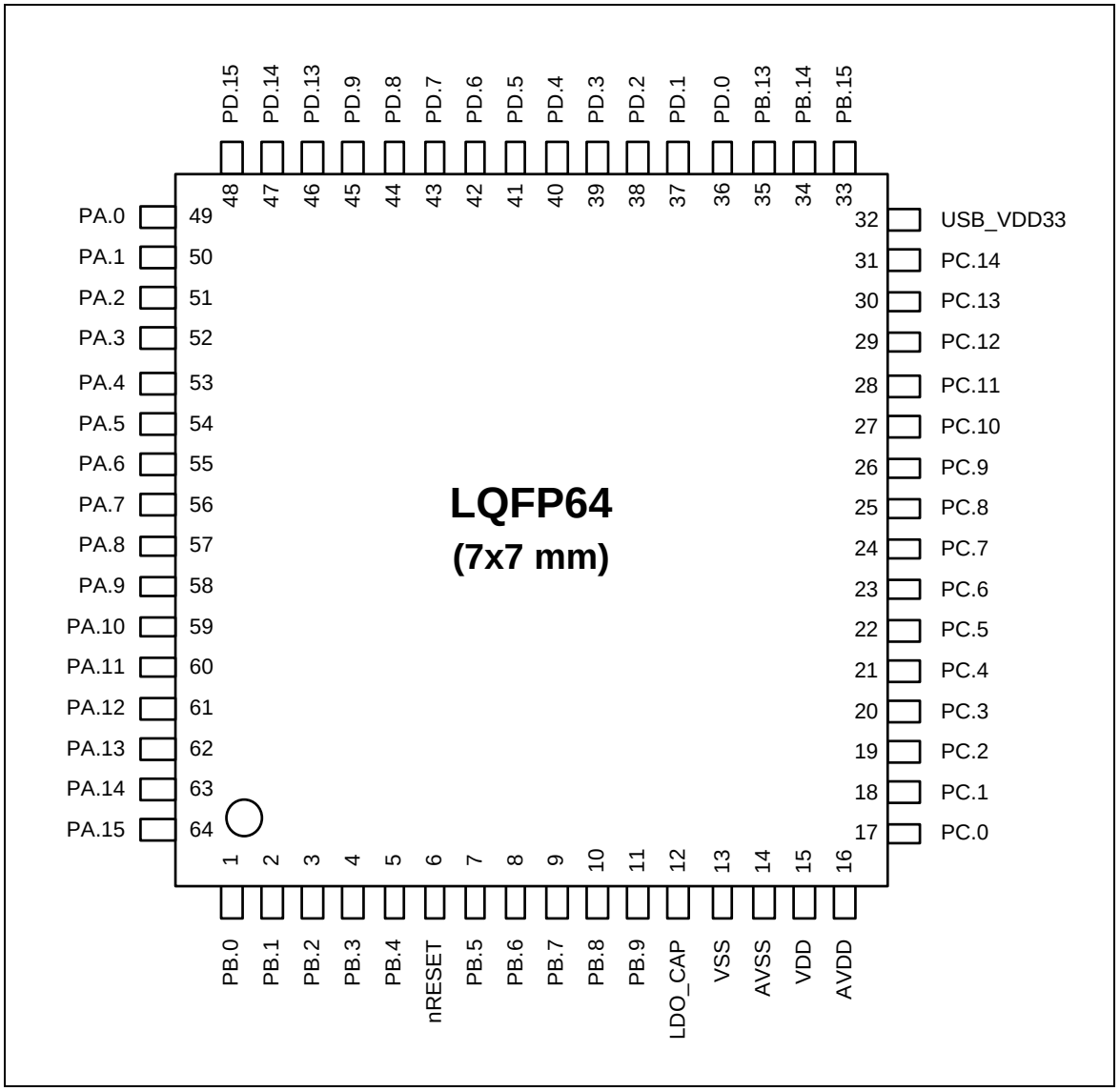


Figure 4.3-2 LQFP64 (7x7 mm) Pin Diagram

4.3.3 LQFP64 (10x10 mm) Pin Diagram

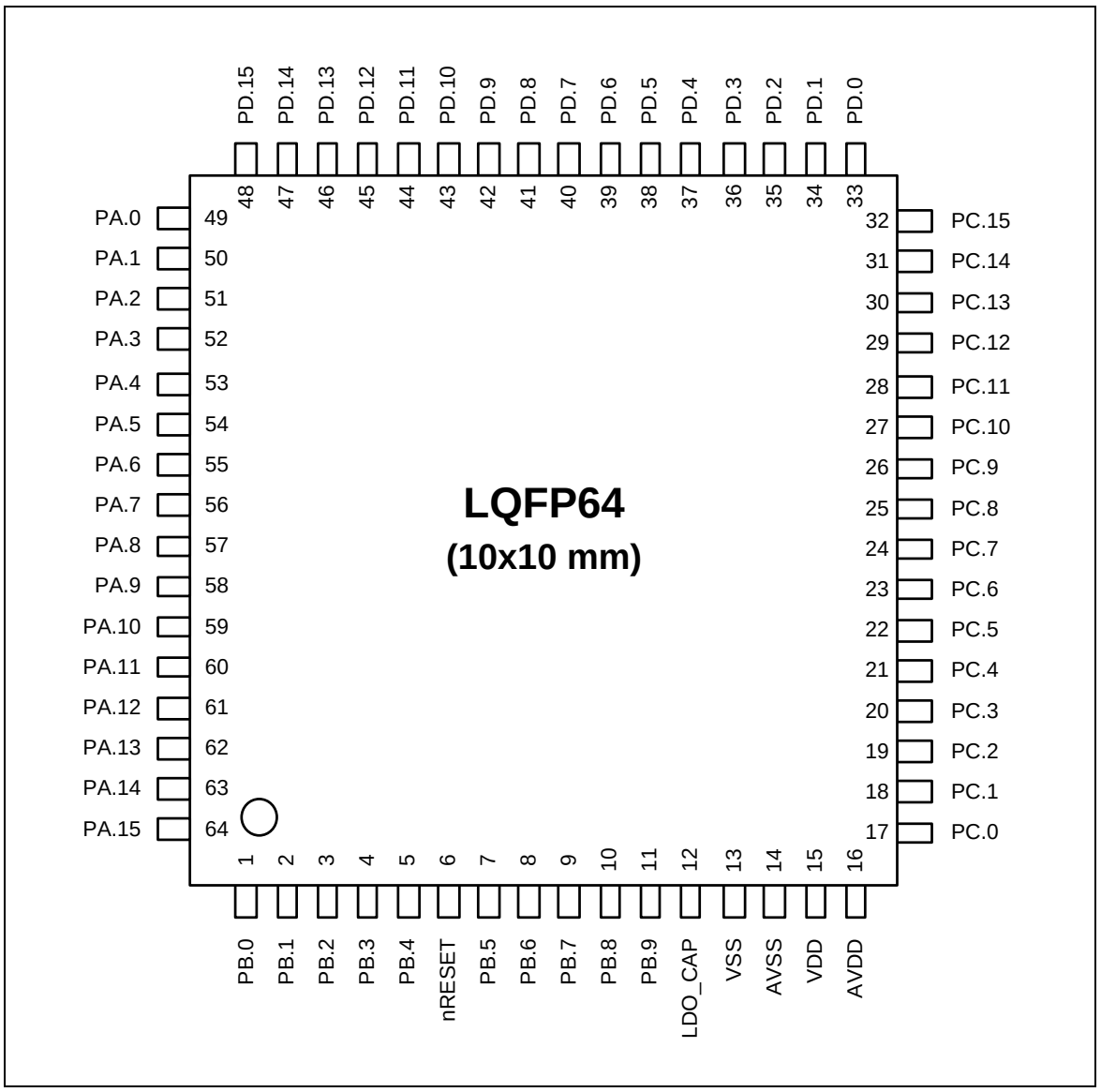


Figure 4.3-3 LQFP64 (10x10 mm) Pin Diagram

4.4 Pin Description

MFP = Multi-function pin.

Note: Pin Type I=Digital Input, O = Digital Output; A = Analog Pin; P = Power Pin;

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
1	1	1	PB.0	I/O	MFP0	General purpose digital I/O pin.
			PWM0_SYNC_IN	I/O	MFP1	PWM0 counter synchronous trigger input pin.
			I2C0_SCL	I/O	MFP2	I2C0 clock pin.
			PWM0_CH0	I/O	MFP3	PWM0 channel0 output/capture input.
2	2	2	PB.1	I/O	MFP0	General purpose digital I/O pin.
			PWM0_SYNC_OUT	I/O	MFP1	PWM0 counter synchronous trigger output pin.
			I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
			PWM0_CH1	I/O	MFP3	PWM0 channel1 output/capture input.
3	3	3	PB.2	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH0	I/O	MFP1	PWM0 channel0 output/capture input.
			TM2	I/O	MFP2	Timer2 event counter input / toggle output.
			PWM0_CH2	I/O	MFP3	PWM0 channel2 output/capture input.
4	4	4	PB.3	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH1	I/O	MFP1	PWM0 channel1 output/capture input.
			TM2_EXT	I/O	MFP2	Timer2 external capture input.
			DMIC_DAT1	I	MFP3	Digital microphone channel 1 data input pin.
			UART0_RXD	I	MFP4	UART0 Data receiver input pin.
			PWM0_CH3	I/O	MFP5	PWM0 channel3 output/capture input.
5	5	5	PB.4	I/O	MFP0	General purpose digital I/O pin.
			UART0_nCTS	I	MFP1	Clear to Send input pin for UART0.
			PWM0_CH0	I/O	MFP2	PWM0 channel0 output/capture input.
			DMIC_CLK1	O	MFP3	Digital microphone channel 1 clock output pin.
			UART0_TXD	O	MFP4	UART0 data transmitter output pin.
			PWM0_CH4	I/O	MFP5	PWM0 channel4 output/capture input.
6	6	6	RESETN	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
7	7	7	PB.5	I/O	MFP0	General purpose digital I/O pin.
			XT1_OUT	I	MFP1	External 4~24.576 MHz (high speed) crystal output pin.
			PWM0_CH1	I/O	MFP2	PWM0 channel1 output/capture input.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
			DMIC_DAT0	I	MFP5	Digital microphone channel 0 data input pin.
8	8	8	PB.6	I/O	MFP0	General purpose digital I/O pin.
			XT1_IN	I	MFP1	External 4~24.576 MHz (high speed) crystal input pin.
			PWM0_CH2	I/O	MFP2	PWM0 channel2 output/capture input.
			I2C0_SCL	I/O	MFP4	I2C0 serial clock pin.
			I2C1_SCL	I/O	MFP5	I2C1 serial clock pin.
			DMIC_CLK0	O	MFP6	Digital microphone channel 0 clock output pin.
	9	9	PB.7	I/O	MFP0	General purpose digital I/O pin.
			UART0_nRTS	O	MFP1	Request to Send output pin for UART0.
			PWM0_CH3	I/O	MFP2	PWM0 channel3 output/capture input.
	10	10	PB.8	I/O	MFP0	General purpose digital I/O pin.
			UART0_TXD	O	MFP1	UART0 Data transmitter output pin.
			PWM0_CH4	I/O	MFP2	PWM0 channel4 output/capture input.
	11	11	PB.9	I/O	MFP0	General purpose digital I/O pin.
			UART0_RXD	I	MFP1	UART0 Data receiver input pin.
			PWM0_CH5	I/O	MFP2	PWM0 channel5 output/capture input.
9	12	12	LDO_CAP	P	MFP0	LDO output pin. Note: This pin needs to be connected with a 1uF capacitor.
10	13	13	VSS	P	MFP0	Ground pin for digital circuit.
11	14	14	AVSS	P	MFP0	Ground pin for analog circuit.
12	15	15	VDD	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
13	16	16	AVDD	P	MFP0	Power supply for internal analog circuit.
14	17	17	PC.0	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SCL	I/O	MPF1	I2C1 clock pin.
			X32_OUT	O	MFP2	External 32.768 kHz (low-speed) crystal output pin.
			SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin; or I2S1 data output pin.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
15	18	18	PC.1	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SDA	I/O	MFP1	I2C1 data input/output pin.
			X32_IN	I	MFP2	External 32.768 kHz (low-speed) crystal input pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin; or I2S1 data input pin.
16	19	19	PC.2	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SMBSUS	O	MFP1	I2C1 SMBus SMBSUS# pin (PMBus CONTROL pin)
			TM3	I/O	MFP2	Timer3 event counter input / toggle output.
			SPI1_CLK	I/O	MFP3	SPI1 Serial Clock pin; or I2S1 bit clock pin.
17	20	20	PC.3	I/O	MFP0	General purpose digital I/O pin.
			I2C1_SMBAL	O	MFP1	I2C1 SMBus SMBALERT# pin
			TM3_EXT	I/O	MFP2	Timer3 external capture input.
			SPI1_SS	I/O	MFP3	SPI1 slave select pin; or I2S1 left right channel clock pin.
18	21	21	PC.4	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH2	I/O	MFP1	PWM0 channel2 output/capture input.
			CLKO	O	MFP2	Clock Output pin.
			SPI1_I2SMCLK	O	MFP3	SPI1 I2S master clock output pin.
	22	22	PC.5	I/O	MFP0	General purpose digital I/O pin.
			INT1	I	MFP1	External interrupt1 input pin.
			SPI2_MOSI	I/O	MFP2	SPI2 MOSI (Master Out, Slave In) pin.
	23	23	PC.6	I/O	MFP0	General purpose digital I/O pin.
			INT2	I	MFP1	External interrupt2 input pin.
			SPI2_MISO	I/O	MFP2	SPI2 MISO (Master In, Slave Out) pin.
	24	24	PC.7	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS0	I/O	MFP1	1st SPI0 Slave Select pin
			SPI2_CLK	I/O	MFP2	SPI2 serial clock pin.
	25	25	PC.8	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	MFP1	2nd SPI0 MOSI (Master Out, Slave In) pin.
			SPI2_SS	I/O	MFP2	SPI2 Slave Select pin.
	26	26	PC.9	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO1	I/O	MFP1	2nd SPI0 MISO (Master In, Slave Out) pin.
			SPI2_I2SMCLK	O	MFP2	SPI2 I2S master clock output pin

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
	27	27	PC.10	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	MFP1	1st SPI0 MOSI (Master Out, Slave In) pin.
			PWM0_BRAKE0	I	MFP2	Brake input pin 0 of PWM0.
			DPWM_RN	O	MFP3	Audio DPWM right channel negative output pin.
	28	28	PC.11	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO0	I/O	MFP1	1st SPI0 MISO (Master In, Slave Out) pin.
			PWM0_BRAKE1	I	MFP2	Brake input pin 1 of PWM0.
			DPWM_RP	O	MFP3	Audio DPWM right channel positive output pin.
	29	29	PC.12	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
			DPWM_LN	O	MFP3	Audio DPWM left channel negative output pin.
	30	30	PC.13	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH3	I/O	MFP1	PWM0 channel3 output/capture input.
			I2C0_SCL	I/O	MFP2	I2C0 clock pin.
			DPWM_LP	O	MFP3	Audio DPWM left channel positive output pin.
	31	31	PC.14	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH4	I/O	MFP1	PWM0 channel4 output/capture input.
			I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
			DPWM_SN	O	MFP3	Audio DPWM sub-woofer channel negative output pin.
		32	PC.15	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS1	O	MFP1	2nd SPI0 Slave Select pin
			DPWM_SP	O	MFP3	Audio DPWM sub-woofer channel positive output pin.
19	32		USB_VDD33	P	MFP0	Power supply for USB, DC 3.3V.
20	33		PB.15	I/O	MFP0	General purpose digital I/O pin.
			USB_VBUS	P	MFP1	Power supply from USB or HUB.
			I2S0_MCLK	O	MFP2	I2S0 master clock output pin.
21	34		PB.14	I/O	MFP0	General purpose digital I/O pin.
			USB_D-	A	MFP1	USB differential signal D-.
			I2S0_DO	O	MFP2	I2S0 data output pin.
22	35		PB.13	I/O	MFP0	General purpose digital I/O pin.
			USB_D+	A	MFP1	USB differential signal D+.
			I2S0_DI	I	MFP2	I2S0 data input pin.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
23	36	33	PD.0	I/O	MFP0	General purpose digital I/O pin.
			INT3	I	MFP1	External interrupt3 input pin.
			I2C1_SCL	I/O	MFP2	I2C1 clock pin.
			I2C0_SCL	I/O	MFP3	I2C0 clock pin.
			I2S0_BCLK	I/O	MFP4	I2S0 bit clock pin.
			DPWM_LN	O	MFP5	Audio DPWM left channel negative output pin.
24	37	34	PD.1	I/O	MFP0	General purpose digital I/O pin.
			INT4	I	MFP1	External interrupt4 input pin.
			I2C1_SDA	I/O	MFP2	I2C1 data p input/output in.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			I2S0_LRCK	I/O	MFP4	I2S0 left right channel clock pin.
			DPWM_LP	O	MFP5	Audio DPWM left channel positive output pin.
25	38	35	PD.2	I/O	MFP0	General purpose digital I/O pin.
			TRACE_CLK	O	MFP1	TPIU for ETM Tx trace clock output pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			I2S0_MCLK	O	MFP3	I2S0 master clock output pin.
			I2C1_SCL	I/O	MFP4	I2C1 clock pin.
			TM0	I/O	MFP5	Timer0 event counter input / toggle output.
26	39	36	PD.3	I/O	MFP0	General purpose digital I/O pin.
			TRACE_DATA0	O	MFP1	TPIU for ETM Tx trace data output bit0.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			I2S0_LRCK	I/O	MFP3	I2S0 left right channel clock pin.
			DMIC_CLK1	O	MFP4	Digital microphone channel 1 clock output pin.
			TM2	I/O	MFP5	Timer2 event counter input / toggle output.
27	40	37	PD.4	I/O	MFP0	General purpose digital I/O pin.
			TRACE_DATA1	O	MFP1	TPIU for ETM Tx trace data output bit1.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			I2S0_DI	I	MFP3	I2S0 data input pin.
			DMIC_DAT1	I	MFP4	Digital microphone channel 1 data input pin.
			TM1	I/O	MFP5	Timer1 event counter input / toggle output.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
28	41	38	PD.5	I/O	MFP0	General purpose digital I/O pin.
			TRACE_DATA2	O	MFP1	TPIU for ETM Tx trace data output bit2.
			SPI1_SS	I/O	MFP2	SPI1 Slave Select pin.
			I2S0_DO	O	MFP3	I2S0 data output pin.
			DMIC_CLK0	O	MFP4	Digital microphone channel 0 clock output pin.
			DPWM_RN	O	MFP5	Audio DPWM right channel negative output pin.
	42	39	PD.6	I/O	MFP0	General purpose digital I/O pin.
			TRACE_DATA3	O	MFP1	TPIU for ETM Tx trace data output bit3.
			SPI1_I2SMCLK	O	MFP2	SPI1 I2S master clock output pin
			I2S0_BCLK	I/O	MFP3	I2S0 Bit Clock pin.
			DMIC_DAT0	I	MFP4	Digital microphone channel 0 data input pin.
			DPWM_RP	O	MFP5	Audio DPWM right channel positive output pin.
	43	40	PD.7	I/O	MFP0	General purpose digital I/O pin.
			PWM0_CH5	I/O	MFP1	PWM0 channel5 output/capture input.
			INT1	I	MFP2	External interrupt1 input pin.
29	44	41	PD.8	I/O	MFP0	General purpose digital I/O pin.
			ICE_CLK	I	MFP1	Serial wired debugger clock pin
			TM0	I/O	MFP2	Timer0 event counter input / toggle output.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
			I2C0_SCL	I/O	MFP4	I2C0 clock pin.
			DPWM_SN	O	MFP5	Audio DPWM sub-woofer channel negative output pin.
30	45	42	PD.9	I/O	MFP0	General purpose digital I/O pin.
			ICE_DAT	I/O	MFP1	Serial wired debugger data pin
			TM0_EXT	I/O	MFP2	Timer0 external capture input.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
			DPWM_SP	O	MFP5	Audio DPWM sub-woofer channel positive output pin.
		43	PD.10	I/O	MFP0	General purpose digital I/O pin.
			INT5	I	MFP1	External interrupt5 input pin.
			EADC0_ST	I	MFP2	EADC0 external trigger input.
		44	PD.11	I/O	MFP0	General purpose digital I/O pin.
			UART0_TXD	O	MFP1	UART0 Data transmitter output pin.
			INT2	I	MFP2	External interrupt2 input pin.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
		45	PD.12	I/O	MFP0	General purpose digital I/O pin.
			UART0_RXD	I	MFP1	UART0 Data receiver input pin.
			INT3	I	MFP2	External interrupt3 input pin.
			PWM0_CH3	I/O	MFP3	PWM0 channel3 output/capture input.
			INT0	I	MFP4	External interrupt0 input pin.
	46	46	PD.13	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS1	O	MFP1	2nd SPI0 Slave Select pin
			EADC0_CH10	A	MFP2	EADC0 channel10 analog input.
31	47	47	PD.14	I/O	MFP0	General purpose digital I/O pin.
			UART0_nCTS	I	MFP1	Clear to Send input pin for UART0.
			EADC0_CH11	A	MFP2	EADC0 channel11 analog input.
			I2C0_SCL	I/O	MFP3	I2C0 clock pin.
			UART0_TXD	O	MFP4	UART0 data transmitter output pin.
			I2C1_SCL	I/O	MFP5	I2C1 clock pin.
32	48	48	PD.15	I/O	MFP0	General purpose digital I/O pin.
			UART0_nRTS	O	MFP1	Request to Send output pin for UART0.
			EADC0_CH12	A	MFP2	EADC0 channel12 analog input.
			I2C0_SDA	I/O	MFP3	I2C0 data input/output pin.
			UART0_RXD	I	MFP4	UART0 data receiver input pin.
			I2C1_SDA	I/O	MFP5	I2C1 data input/output pin.
33	49	49	PA.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS1	O	MFP1	2nd SPI0 Slave Select pin
			EADC0_CH0	A	MFP2	EADC0 channel0 analog input.
			DMIC_DAT0	I	MFP3	Digital microphone channel 0 data input pin.
34	50	50	PA.1	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI1	I/O	MFP1	2nd SPI0 MOSI (Master Out, Slave In) pin.
			EADC0_CH1	A	MFP2	EADC0 channel1 analog input.
			DMIC_CLK0	O	MFP3	Digital microphone channel 0 clock output pin.
35	51	51	PA2	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO1	I/O	MFP1	2nd SPI0 MISO (Master In, Slave Out) pin.
			EADC0_CH2	A	MFP2	EADC0 channel2 analog input.
			DMIC_DAT1	I	MFP3	Digital microphone channel 1 data input pin.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
36	52	52	PA.3	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MOSI0	I/O	MFP1	1st SPI0 MOSI (Master Out, Slave In) pin.
			EADC0_CH3	A	MFP2	EADC0 channel3 analog input.
			DMIC_CLK1	O	MFP3	Digital microphone channel 1 clock output pin.
37	53	53	PA.4	I/O	MFP0	General purpose digital I/O pin.
			SPI0_MISO0	I/O	MFP1	1st SPI0 MISO (Master In, Slave Out) pin.
			EADC0_CH4	A	MFP2	EADC0 channel4 analog input.
			DPWM_LN	O	MFP3	Audio DPWM left channel negative output pin.
38	54	54	PA.5	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP1	SPI0 serial clock pin.
			EADC0_CH5	A	MFP2	EADC0 channel5 analog input.
			DPWM_LP	O	MFP3	Audio DPWM left channel positive output pin.
39	55	55	PA.6	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS0	I/O	MFP1	1st SPI0 Slave Select pin
			EADC0_CH6	A	MFP2	EADC0 channel6 analog input.
40	56	56	PA.7	I/O	MFP0	General purpose digital I/O pin.
			UART0_TXD	O	MFP1	UART0 data transmitter output pin.
			EADC0_CH7	A	MFP2	EADC0 channel7 analog input.
			SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin; or I2S2 data input pin.
41	57	57	PA.8	I/O	MFP0	General purpose digital I/O pin.
			UART0_RXD	I	MFP1	UART0 data receiver input pin..
			EADC0_CH8	A	MFP2	EADC0 channel8 analog input.
			SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin; or I2S2 data output pin.
42	58	58	PA.9	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SCL	I/O	MFP1	I2C0 Serial Clock pin
			EADC0_CH9	A	MFP2	EADC0 channel9 analog input.
			SPI2_SS	I/O	MFP4	SPI2 slave select pin; or I2S2 left right channel clock pin.
43	59	59	PA.10	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SDA	I/O	MFP1	I2C0 data input/output pin.
			EADC0_ST	I	MFP2	EADC0 external trigger input.
			DPWM_RN	O	MFP3	Audio DPWM right channel negative output pin.
			SPI2_CLK	I/O	MFP4	SPI2 clock pin; or I2S2 bit clock pin.

Pins			Pin Name	Type	MFP	Description
QFN48 (6x6)	LQFP64 (7x7)	LQFP64 (10x10)				
44	60	60	PA.11	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SMBSUS	O	MFP1	I2C0 SMBus SMBSUS# pin (PMBus CONTROL pin)
			TM0	I/O	MFP2	Timer0 event counter input / toggle output.
			DPWM_RP	O	MFP3	Audio DPWM right channel positive output pin.
45	61	61	PA.12	I/O	MFP0	General purpose digital I/O pin.
			I2C0_SMBAL	O	MFP1	I2C0 SMBus SMBALERT# pin
			TM0_EXT	I/O	MFP2	Timer0 external capture input.
			SPI2_I2SMCLK	O	MFP4	SPI2 I2S master clock output pin.
46	62	62	PA.13	I/O	MFP0	General purpose digital I/O pin.
			CLKO	O	MFP1	Clock Output pin.
			INT0	I	MFP2	External interrupt0 input pin.
			DPWM_SN	O	MFP3	Audio DPWM sub-woofer channel negative output pin.
			I2C1_SCL	I/O	MFP4	I2C1 clock pin.
47	63	63	PA.14	I/O	MFP0	General purpose digital I/O pin.
			SPI0_SS0	I/O	MFP1	1st SPI0 Slave Select pin
			TM1	I/O	MFP2	Timer1 event counter input / toggle output.
			DPWM_SP	O	MFP3	Audio DPWM sub-woofer channel positive output pin.
			I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
48	64	64	PA.15	I/O	MFP0	General purpose digital I/O pin.
			INT0	I	MFP1	External interrupt0 input pin.
			TM1_EXT	I/O	MFP2	Timer1 external capture input.

Table 4.4-1 Pin Description

4.5 GPIO Alternate Function Summary

MFP* = Multi-function pin. (Reference section)

Pin function is defined in SYS_GPx_MFPx registers. For example PA0~7 pin functions are defined in SYS_GPA_MFPL register, and PA8~15 pin functions are defined in SYS_GPA_MFPH register.

MFP0	MFP1	MFP2	MFP3	MFP4	MFP5
PA.0	SPI0_SS1	EADC0_CH0	DMIC_DAT0		
PA.1	SPI0_MOSI1	EADC0_CH1	DMIC_CLK0		
PA.2	SPI0_MISO1	EADC0_CH2	DMIC_DAT1		
PA.3	SPI0_MOSI0	EADC0_CH3	DMIC_CLK1		
PA.4	SPI0_MISO0	EADC0_CH4	DPWM_LN		
PA.5	SPI0_CLK	EADC0_CH5	DPWM_LP		
PA.6	SPI0_SS0	EADC0_CH6			
PA.7	UART0_TXD	EADC0_CH7		SPI2_MISO	
PA.8	UART0_RXD	EADC0_CH8		SPI2_MOSI	
PA.9	I2C0_SCL	EADC0_CH9		SPI2_SS	
PA.10	I2C0_SDA	EADC0_ST	DPWM_RN	SPI2_CLK	
PA.11	I2C0_SMBSUS	TM0	DPWM_RP		
PA.12	I2C0_SMBAL	TM0_EXT		SPI2_I2SMCLK	
PA.13	CLKO	INT0	DPWM_SN	I2C1_SCL	
PA.14	SPI0_SS0	TM1	DPWM_SP	I2C1_SDA	
PA.15	INT0	TM1_EXT			
PB.0	PWM0_SYNC_IN	I2C0_SCL	PWM0_CH0		
PB.1	PWM0_SYNC_OUT	I2C0_SDA	PWM0_CH1		
PB.2	PWM0_CH0	TM2	PWM0_CH2		
PB.3	PWM0_CH1	TM2_EXT	DMIC_DAT1	UART0_RXD	PWM0_CH3
PB.4	UART0_nCTS	PWM0_CH0	DMIC_CLK1	UART0_TXD	PWM0_CH4
PB.5	XT1_OUT	PWM0_CH1	I2C0_SDA	I2C1_SDA	DMIC_DAT0
PB.6	XT1_IN	PWM0_CH2	I2C0_SCL	I2C1_SCL	DMIC_CLK0
PB.7	UART0_nRTS	PWM0_CH3			
PB.8	UART0_TXD	PWM0_CH4			
PB.9	UART0_RXD	PWM0_CH5			
PB.13	USB_D+	I2S0_DI			
PB.14	USB_D-	I2S0_DO			
PB.15	USB_VBUS	I2S0_MCLK			
PC.0	I2C1_SCL	X32_OUT	SPI1_MOSI		
PC.1	I2C1_SDA	X32_IN	SPI1_MISO		

MFP0	MFP1	MFP2	MFP3	MFP4	MFP5
PC.2	I2C1_SMBSUS	TM3	SPI1_CLK		
PC.3	I2C1_SMBAL	TM3_EXT	SPI1_SS		
PC.4	PWM0_CH2	CLKO	SPI1_I2SMCLK		
PC.5	INT1	SPI2_MOSI			
PC.6	INT2	SPI2_MISO			
PC.7	SPI0_SS0	SPI2_CLK			
PC.8	SPI0_MOSI1	SPI2_SS			
PC.9	SPI0_MISO1	SPI2_I2SMCLK			
PC.10	SPI0_MOSI0	PWM0_BRAKE0	DPWM_RN		
PC.11	SPI0_MISO0	PWM0_BRAKE1	DPWM_RP		
PC.12	SPI0_CLK		DPWM_LN		
PC.13	PWM0_CH3	I2C0_SCL	DPWM_LP		
PC.14	PWM0_CH4	I2C0_SDA	DPWM_SN		
PC.15	SPI0_SS1		DPWM_SP		
PD.0	INT3	I2C1_SCL	I2C0_SCL	I2S0_BCLK	DPWM_LN
PD.1	INT4	I2C1_SDA	I2C0_SDA	I2S0_LRCK	DPWM_LP
PD.2	TRACE_CLK	SPI1_MOSI	I2S0_MCLK	I2C1_SCL	TM0
PD.3	TRACE_DATA0	SPI1_MISO	I2S0_LRCK	DMIC_CLK1	TM2
PD.4	TRACE_DATA1	SPI1_CLK	I2S0_DI	DMIC_DAT1	TM1
PD.5	TRACE_DATA2	SPI1_SS	I2S0_DO	DMIC_CLK0	DPWM_RN
PD.6	TRACE_DATA3	SPI1_I2SMCLK	I2S0_BCLK	DMIC_DAT0	DPWM_RP
PD.7	PWM0_CH5	INT1			
PD.8	ICE_CLK	TM0	I2C1_SCL	I2C0_SCL	DPWM_SN
PD.9	ICE_DAT	TM0_EXT	I2C1_SDA	I2C0_SDA	DPWM_SP
PD.10	INT5	EADC0_ST			
PD.11	UART0_TXD	INT2			
PD.12	UART0_RXD	INT3	PWM0_CH3	INT0	
PD.13	SPI0_SS1	EADC0_CH10			
PD.14	UART0_nCTS	EADC0_CH11	I2C0_SCL	UART0_TXD	I2C1_SCL
PD.15	UART0_nRTS	EADC0_CH12	I2C0_SDA	UART0_RXD	I2C1_SDA

Table 4.5-1 GPIO Alternate Function Summary

5 BLOCK DIAGRAM

5.1 ISD94100 Series Block Diagram

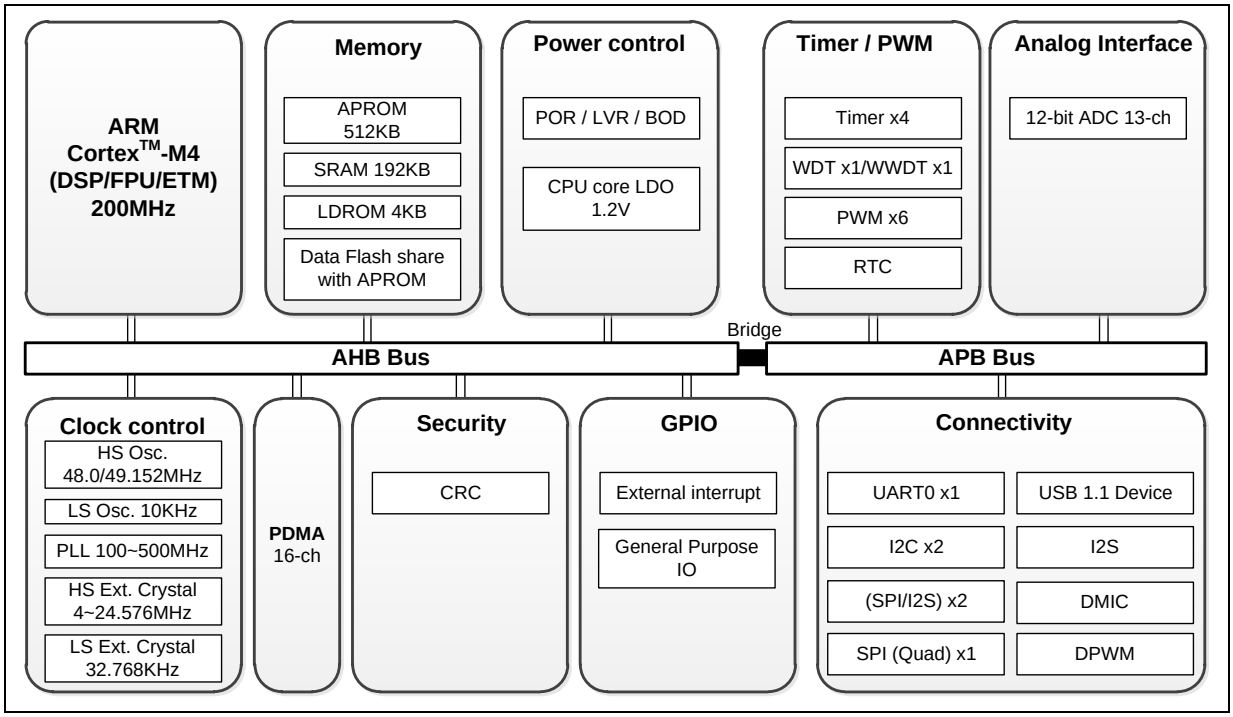


Figure 5.1-1 ISD94100 Series Block Diagram

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

6.1.1 Voltage Characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}– V_{SS}	DC Power Supply	-0.3	+3.6	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
$\|V_{SS} – AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance GPIO	-	5.5	V
	Input voltage on any other pin[2]	-	V_{DD}	V

Note:

1. Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the life and reliability of the device.
2. Non 5V-tolerance PIN: PA0 ~ PA15, PB5, PB6, PC0 and PC1.

Table 6.1.1-1 Voltage characteristics

6.1.2 Current Characteristics

Symbol	Parameter	Min	Max	Unit
– I_{DD}	Maximum Current into V_{DD}	-	200	mA
I_{SS}	Maximum Current out of V_{SS}	-	100	
I_{IO}	Maximum Current sunk by a I/O pin	-	20	
	Maximum Current sourced by a I/O pin	-	20	
	Maximum Current sunk by total I/O pins	-	100	
	Maximum Current sourced by total I/O pins	-	100	

Table 6.1.2-1 Current characteristics

6.1.3 Thermal Characteristics

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	

Table 6.1.3-1 Thermal characteristics

6.2 General Operating Conditions

(V_{DD} - V_{SS} = 1.8 ~ 3.3 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{HCLK}	Internal AHB Clock Frequency	-	-	200	MHz	
V_{DD}	Typical Operation Voltage	1.8[1]	-	3.3[1]	V	
AV_{DD}	Analong Operation Voltage	V_{DD}			V	
USB_V_{DD33}	USB Operation Voltage	3.0	-	3.6	V	
V_{LDO}	LDO Output Voltage		1.2		V	Normal mode
C_{LDO}	LDO Output Capacitance on LDO_CAP Pin	-	1	-	uF	

Note:

1. The limitation of V_{DD} operation voltage is 1.62V ~ 3.6V.

Table 6.2-1 General Operating Conditions

6.3 DC Electrical Characteristics

(V_{DD} - V_{SS} = 1.8 ~ 3.3 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD5}	Operating Current Normal Run Mode HCLK = 49.152 MHz while(1){} executed from flash	-	10	16	mA	V_{DD}	3.3 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD6}		-	8	12	mA	V_{DD}	3.3 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD7}		-	10	16	mA	V_{DD}	1.8 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD8}		-	8	12	mA	V_{DD}	1.8 V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD5}	Operating Current Normal Run Mode HCLK =12 MHz while(1){} executed from flash	-	5	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD6}		-	3.2	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD7}		-	4.8	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD8}		-	3	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD9}	Operating Current Normal Run Mode HCLK = 160 MHz while(1){} executed from flash	-	31	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled
I_{DD10}		-	21	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Disabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD11}		-	30.5	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled
I_{DD12}		-	20.7	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160M
						All digital modules	Disabled
I_{DD9}	Operating Current Normal Run Mode HCLK = 200 MHz while(1){} executed from flash	-	39	-	mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{DD10}		-	26.6	-	mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled
I_{DD11}		-	38.5	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{DD12}		-	26.3	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{DD13}	Operating Current Normal Run Mode HCLK =4 MHz while(1){} executed from flash	-	3.5	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD14}		-	2.4	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{DD15}		-	3.2	-	mA	V_{DD}	1.8V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{DD16}		-	2	-	mA	V_{DD}	1.8V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE1}	Operating Current Idle Mode HCLK = 49.152 MHz	-	6.1	10	mA	V_{DD}	3.3V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE2}	Operating Current Idle Mode HCLK =12 MHz	-	2.8	6	mA	V_{DD}	3.3V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE3}		-	6.1	10	mA	V_{DD}	1.8V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE4}		-	2.8	6	mA	V_{DD}	1.8V
						HXT_GM	Disabled
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE5}		-	3.5	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE6}		-	2.3	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE7}	Operating Current Idle Mode HCLK =160 MHz	-	3.4	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE8}		-	2.1	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Enabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE9}		-	19.6	-	mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled
I_{IDLE10}			8.5		mA	V_{DD}	3.3V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Disabled
I_{IDLE11}		-	19.4	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE12}		-	8.3	-	mA	V_{DD}	1.8V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	160 MHz
						All digital modules	Disabled
I_{IDLE9}	Operating Current Idle Mode HCLK =200 MHz	-	24.9	-	mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{IDLE10}			10.6		mA	V_{DD}	3.3 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled
I_{IDLE11}		-	24.5	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Enabled
I_{IDLE12}		-	10.3	-	mA	V_{DD}	1.8 V
						HXT_GM	12 MHz
						HIRC	Disabled
						PLL	200 MHz
						All digital modules	Disabled
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.6	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions	
I_{IDLE14}		-	2	-	mA	V_{DD}	3.3V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{IDLE15}		-	2.3	-	mA	V_{DD}	1.8V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Enabled
I_{IDLE16}		-	1.7	-	mA	V_{DD}	1.8V
						HXT_GM	4 MHz
						HIRC	Disabled
						PLL	Disabled
						All digital modules	Disabled
I_{PWD1}	Power-down Mode (PD)	-	700	3500	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD2}		-	700	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD1}	Low Leakage Power-down Mode (LLPD)	-	350	1500	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD2}		-	350	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD1}	Standby Current Power-down Mode (SPD0 SRAM retention)	-	25	70	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD2}		-	25	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD1}	Standby Current Power-down Mode (SPD1)	-	15	46	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD2}		-	15	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on	
I_{PWD1}	Deep Power-down Mode (DPD)	-	2	6	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on USB_VDD33 pin floating.	
I_{PWD2}		-	2	-	µA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on USB_VDD33 pin floating.	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{PWD3}		-	3.5	7.5	μA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off. LIRC on
I_{PWD4}		-	3.5	-	μA	V_{DD} = 1.8 V, All oscillators and analog blocks turned off. LIRC on
I_{LK}	Input Leakage Current	-1	-	+1	μA	V_{DD} = 3.6 V, 0 < V_{IN}< V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage (TTL input)	-0.3	-	0.8	V	V_{DD} = 3.3 V
		-0.3	-	0.6		V_{DD} = 1.8 V
V_{IH1}	Input High Voltage (TTL input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 3.3 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 1.8 V
V_{ILS}	Negative going threshold (Schmitt input), nRESET	-0.3	-	0.3 V_{DD}	V	
V_{IHS}	Positive going threshold (Schmitt input), nRESET	0.7 V_{DD}	-	V_{DD} + 0.3	V	
R_{RST}	Internal nRESET pin pull up resistor	-	50	-	kΩ	
V_{ILS}	Schmitt input high voltage		0.6* V_{DD}	0.75* V_{DD}	V	
V_{IHS}	Schmitt input low voltage	0.3* V_{DD}	0.4* V_{DD}		V	
Hysteresis	Schmitt buffer hysteresis	-	0.2 V_{DD}	-	V	
I_{SR11}	Source Current (Quasi-bidirectional Mode)	-	-9.3	-	μA	V_{DD} = 3.3 V, V_S = 2.8 V
I_{SR12}		-	-7.5	-	μA	V_{DD} = 2.7 V, V_S = 2.3 V
I_{SR13}		-	-5.6	-	μA	V_{DD} = 1.8 V, V_S = 1.5 V
I_{SR21}	Source Current (Push-pull Mode)	-	-20	-	mA	V_{DD} = 3.3 V, V_S = 2.8 V
I_{SR22}		-14	-15	-	mA	V_{DD} = 2.7 V, V_S = 2.3 V
I_{SR23}		-11	-7.9	-	mA	V_{DD} = 1.8 V, V_S = 1.5 V
I_{SK11}	Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode)	14	20	-	mA	V_{DD} = 3.3 V, V_S = 0.5 V
I_{SK12}		11	15	-	mA	V_{DD} = 2.7 V, V_S = 0.4 V
I_{SK13}		-	8.2	-	mA	V_{DD} = 1.8 V, V_S = 0.3 V

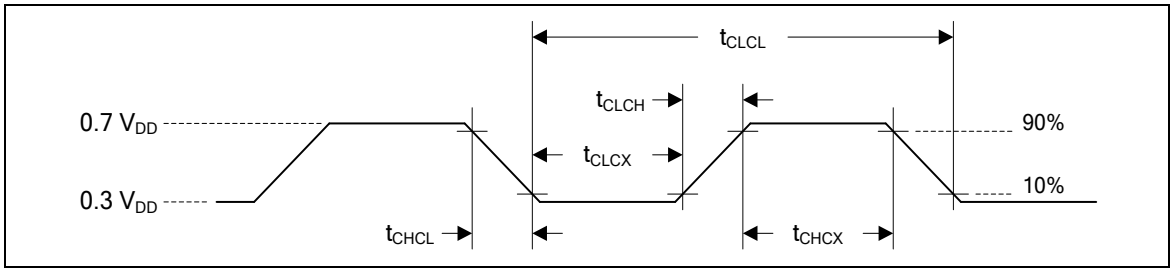
Notes:

1. nRESET pin is a Schmitt trigger input.

Table 6.3-1 DC Electrical Characteristics

6.4 AC Electrical Characteristics

6.4.1 External High Speed Crystal (HXT) Characteristics



Note:

1. Duty cycle is 50%.
2. Guaranteed by design, not tested in production

Figure 6.4-1 External High Speed Crystal Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

Table 6.4.1-1 External High Speed Clock Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{HXT}	Operation Temperature	-40	25	85	℃	-
f_{HXT}	Oscillator Frequency	4	12	24.576	MHz	
I_{HXT}	Operating Current	-	0.37	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 4 MHz T_A = 25 ℃, GM TYPE
		-	0.5	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 12 MHz T_A = 25 ℃, GM TYPE
		-	0.66	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 16 MHz T_A = 25 ℃, GM TYPE
		-	0.84	-	mA	V_{DD} = 3.3V, f_{HXTAL} =24 MHz T_A = 25 ℃, GM TYPE
		-	0.57	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 4 MHz T_A = 25 ℃, INV TYPE
		-	1.4	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 12 MHz T_A = 25 ℃, INV TYPE
		-	2.1	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 16 MHz T_A = 25 ℃, INV TYPE

		-	2.8	-	mA	V_{DD} = 3.3V, f_{HXTAL} = 24 MHz T_A = 25 ℃, INV TYPE

Note:

1. This table is guaranteed by characteristics result, not tested in production.

Table 6.4.1-2 External High Speed Crystal (HXT) Characteristics

6.4.1.1 HXT Typical Crystal Application Circuit

CRYSTAL	C_1	C_2
4 MHz ~ 24.576 MHz	Optional (depending on the crystal specification)	

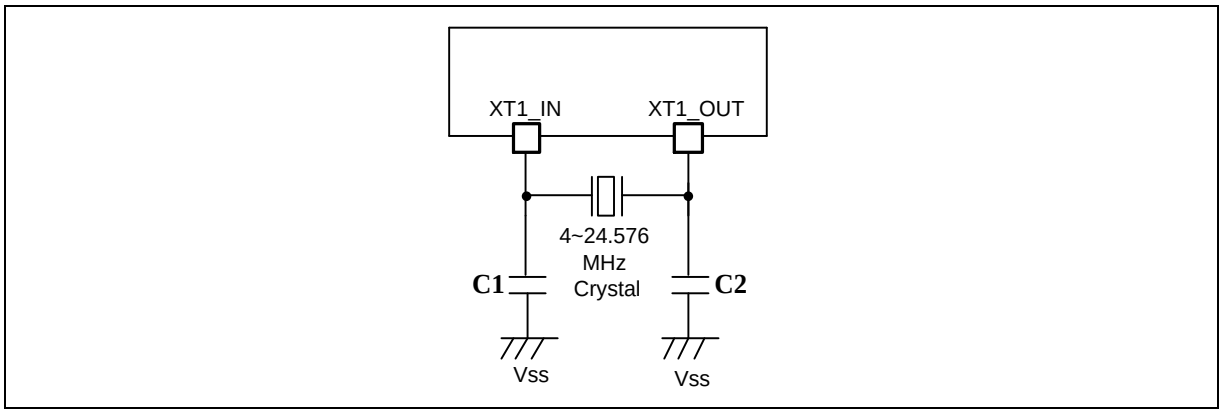


Figure 6.4-2 HXT Typical Crystal Application Circuit

6.4.2 Internal High Speed RC Oscillator (HIRC) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{HRC}	Operation Temperature	-40	25	85	℃	-
f_{HRC}	Center Frequency	-	49.152		MHz	-
	Calibrated Internal Oscillator Frequency	-	±0.25	-	%	T_A = 25 ℃ V_{DD} = 3.3 V
		-3	-	+3	%	T_A = -40℃~ 85 ℃
I_{HRC}	Operating Current	-	200	-	μA	T_A = 25 ℃,V_{DD} = 3.3 V

Table 6.4.2-1 Internal High Speed RC Oscillator (HIRC) Characteristics

6.4.3 External Low Speed Crystal (LXT) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{LXT}	Operation Temperature	-40	25	85	℃	-
f_{LXT}	Oscillator Frequency	-	32.768		kHz	
I_{LXT}	Operating Current	-	0.8	-	μA	T_A = 25 ℃, V_{DD} = 3.3 V
T_S	Stable Time		300	500	ms	

Table 6.4.3-1 External Low Speed Crystal (LXT) Characteristics

6.4.3.1 LXT Typical Crystal Application Circuit

CRYSTAL	C_1	C_2
32.768 kHz	Optional (depending on the crystal specification)	

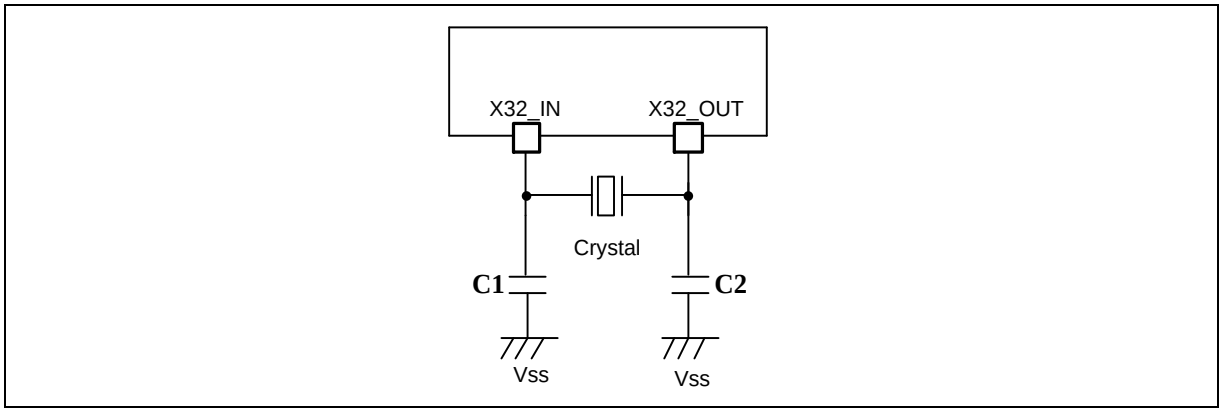


Figure 6.4-3 LXT Typical Crystal Application Circuit

6.4.4 Internal Low Speed RC Oscillator (LIRC) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{LRC}	Operation Temperature	-40	25	85	℃	-
f_{LRC}	Center Frequency	5	10	15	KHz	-
I_{LRC}	Operating Current	-	500	-	nA	T_A = 25 ℃, V_{DD} = 3.3 V

Table 6.4.4-1 Internal Low Speed RC Oscillator (LIRC) Characteristics

6.5 Analog Characteristics

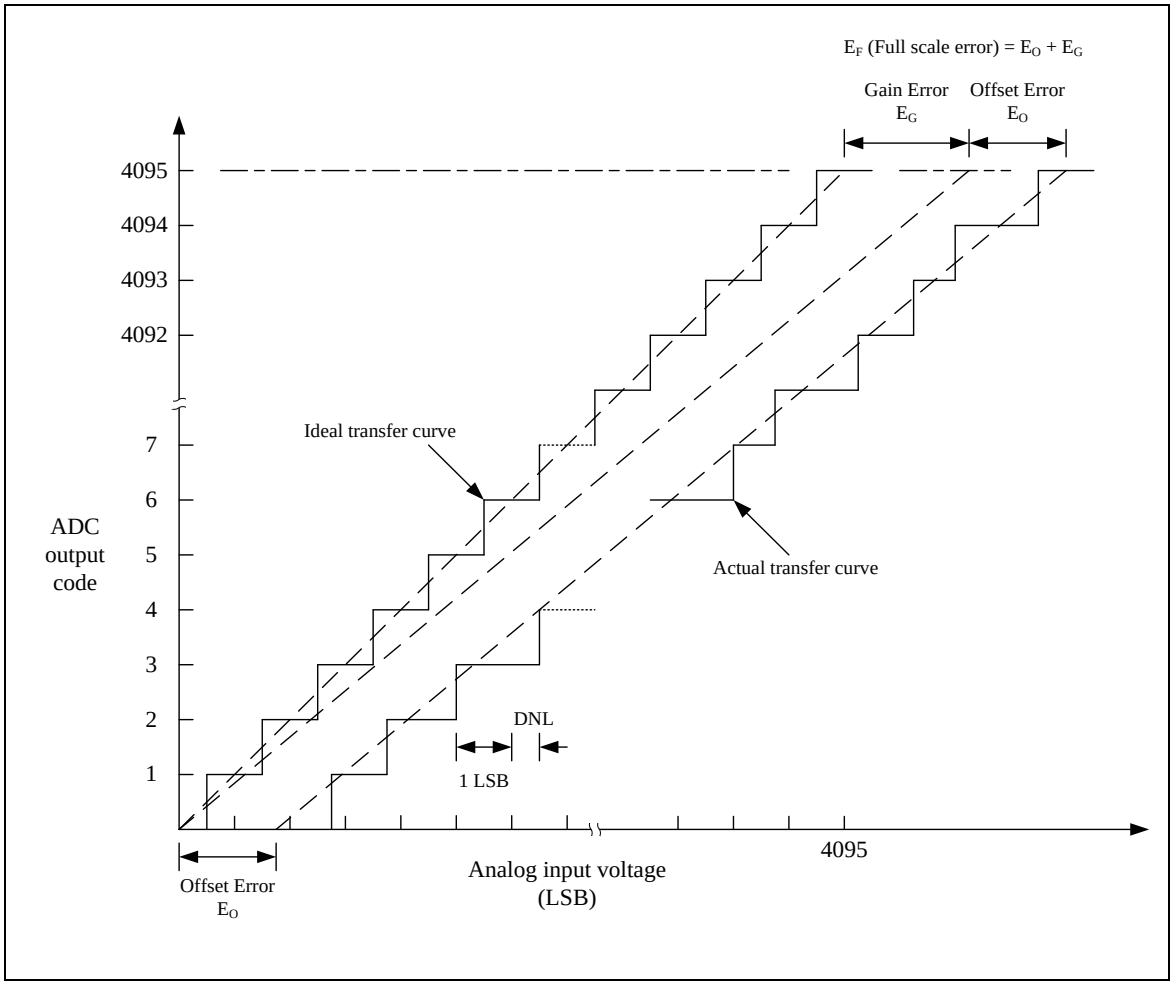
6.5.1 12-bit SARADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution		12		Bit	-
DNL	Differential Nonlinearity Error	-	-	±2	LSB	2MSPS
INL	Integral Nonlinearity Error	-	-	±4	LSB	2MSPS
E_O	Offset Error	-	2	-	LSB	2MSPS
E_G	Gain Error (Transfer Gain)	-	-3	-	LSB	2MSPS
E_A	Absolute Error	-	6	-	LSB	2MSPS
-	Monotonic		Guaranteed		-	-
F_{ADC}	ADC Clock Frequency	0.14	-	60	MHz	AV_{DD} = 1.8~3.6 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	2000	kSPS	AV_{DD} = 1.8~3.6 V
T_{ACQ}	Acquisition Time (Sample Stage)		2~9		$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time		16~23		$1/F_{ADC}$	-
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	6	-	pF	-

Note:

1. This table is guaranteed by characteristics result, not tested in production.
2. The condition is that the error in a conversion started after ADC enable is less than ±0.5 LSB. The reference and input signal are already settled.

Table 6.5.1-1 12-bit SARADC Characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

6.5.2 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{LDO1}	Output Voltage	1.176	1.2	1.224	V	Normal mode
V_{LDO2}	Output Voltage		0.9		V	Low power mode
V_{LDO3}	Output Voltage		1.26		V	Over voltage mode

Notes:

1. It is critical that a 0.1 µF capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. To ensure power stability, a 1uF capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

Table 6.5.2-1 LDO Characteristics

6.5.3 Low Voltage Reset and Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
I_{BOD}	Operating Current	-	60		µA	V_{DD} = 3.6V
V_{BOD_F}	Brown-out Detect Level (Falling edge)	1.50	1.60	1.70	V	BODVL [2:0]=000
		1.70	1.80	1.90	V	BODVL [2:0]=001
		1.90	2.00	2.10	V	BODVL [2:0]=010
		2.10	2.20	2.30	V	BODVL [2:0]=011
		2.30	2.40	2.50	V	BODVL [2:0]=100
		2.50	2.60	2.70	V	BODVL [2:0]=101
		2.70	2.80	2.90	V	BODVL [2:0]=110
		2.90	3.00	3.10	V	BODVL [2:0]=111
V_{BOD_R}	Brown-out Detect Level (Rising edge)	-	V_{BOD_F} + V_{HYS_BOD}	-		
V_{HYS_BOD}	Hysteresis	-	80	-	mV	-
V_{LVR}	Low Voltage Reset Voltage	1.45	1.5	1.55	V	-

Table 6.5.3-1 Low Voltage Reset and Brown-out Detector Characteristics

6.5.4 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Power-on Reset Voltage		1.45		V	-
V_{PORHYS}	Power-on Reset Hysteresis	-	110	-	mV	-
RR_{VDD}	VDD Raising Rate to Ensure Power-on Reset	0.01	-	-	ms/V	-
FR_{VDD}	VDD Falling Rate to Ensure Power-on Reset	0.5	-	-	ms/V	-

Table 6.5.4-1 Power-on Reset Characteristics

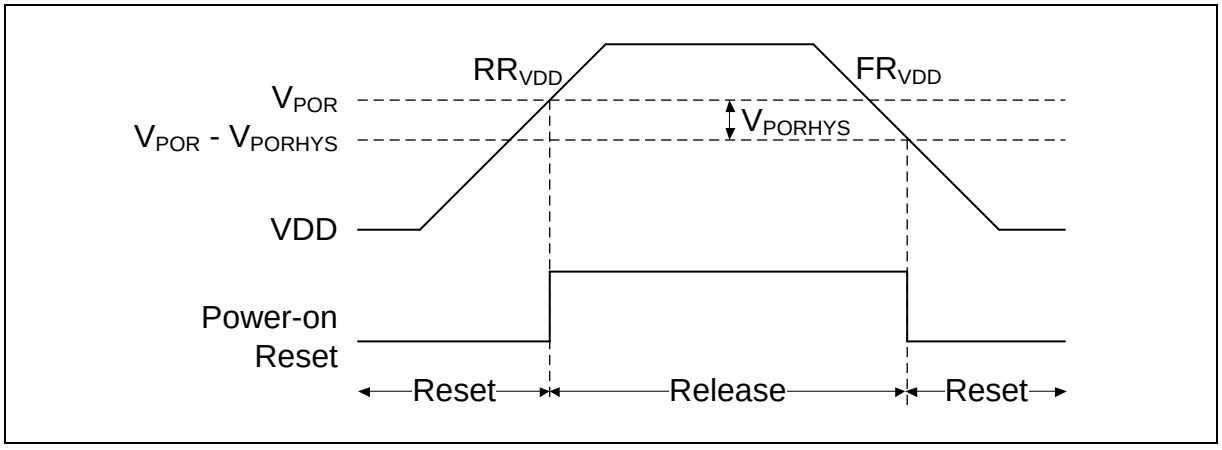


Figure 6.5-1 Power-on Reset Condition

6.6 USB Characteristics

6.6.1 USB Full-Speed Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input High (driven)	2.0	-	-	V	-
V_{IL}	Input Low	-	-	0.8	V	-
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended Receiver Threshold	0.8	-	2.0	V	-
	Receiver Hysteresis	-	200	-	mV	-
V_{OL}	Output Low (driven)	0	-	0.3	V	-
V_{OH}	Output High (driven)	2.8	-	3.6	V	-
V_{CRS}	Output Signal Cross Voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up Resistor		1.2		kΩ	-
Z_{DRV}	Driver Output Resistance	-	10	-	Ω	Steady state drive*
C_{IN}	Transceiver Capacitance	-	-	20	pF	Pin to GND

*Driver output resistance doesn't include series resistor resistance.

Table 6.6.1-1 USB Full-Speed Characteristics

6.6.2 USB Full-Speed PHY Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{FR}	Rise Time	4	-	20	ns	C_L=50p
T_{FF}	Fall Time	4	-	20	ns	C_L=50p
T_{FRFF}	Rise and Fall Time Matching	90	-	111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

Table 6.6.2-1 USB Full-Speed PHY Characteristics

6.6.3 USB VBUS Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{BUS}	VBUS Pin Input Voltage	4.4	5.0	5.25	V	-

Table 6.6.3-1 USB VBUS Characteristics

6.7 VAD Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{VADIDLE}$	Operation Current Idle mode with VAD	-	1.25	-	mA	VDDA = VDD = 3.3 V HCLK = 3.072MHz (HIRC/16) DMIC_MCLK = 1.536 MHz (HIRC/32) DMIC_CLK = 384 kHz (DMIC_MCLK/4) Sample Rate = 8 kHz (Down sample 48) No load

Table 6.7-1 VAD Characteristics

Note: This table is guaranteed by characteristics result, not tested in production.

6.8 Flash DC Electrical Characteristic

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply Voltage	1.08	-	1.32	V	T_A = 25 ℃
N_{ENDUR}	Endurance	10000	-	-	cycles[2]	
T_{RET}	Data Retention	10	-	-	year	
T_{ERASE}	Page Erase Time	92	-	160	ms	
T_{MER}	Mass Erase Time	300	-	350	ms	
T_{PROG}	Program Time	42	-	50	us	
I_{DD1}	Read Current	-	-	4.12	mA	
I_{DD2}	Program Current	-	-	5	mA	
I_{DD3}	Erase Current	-	-	5	uA	

Notes:

1. VFLA is source from chip LDO output voltage.
2. Number of program/erase cycles.
3. This table is guaranteed by design, not test in production.

Table 6.8-1 Flash DC Electrical Characteristics

6.9 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 6.9-1 I²C Dynamic Characteristics

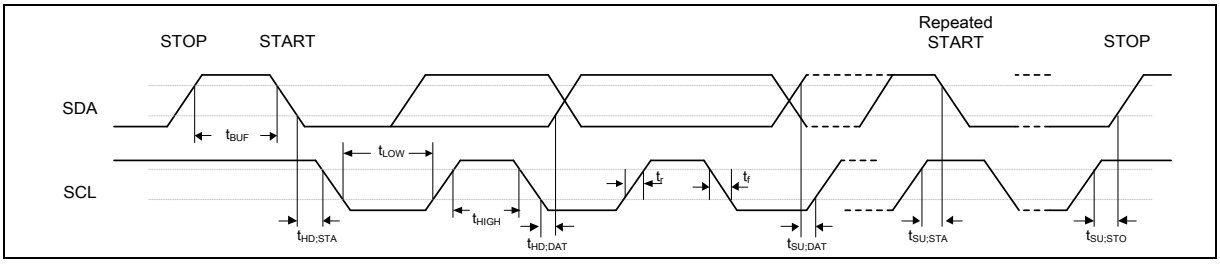


Figure 6.9-1 I²C Timing Diagram

6.10 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (VDD = 1.8 V~3.6V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20 MHz	22.5	-	27.5	ns
t_{DS}	Data input setup time	2	-	-	ns
$t_{H(MI)}$	Data input hold time	4	-	-	ns
t_V	Data output valid time	-	-	1	ns
$t_{H(MO)}$	Data output hold time	0	-	-	ns
SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20 MHz	22.5	-	27.5	ns
t_{DS}	Data input setup time	2			ns
$t_{H(MI)}$	Data input hold time	4			ns
t_V	Data output valid time		-	1	ns
$t_{H(MO)}$	Data output hold time	0	-	-	ns

Table 6.6.3-1 Dynamic Characteristics of Data Input and Output Pin in Master Mode

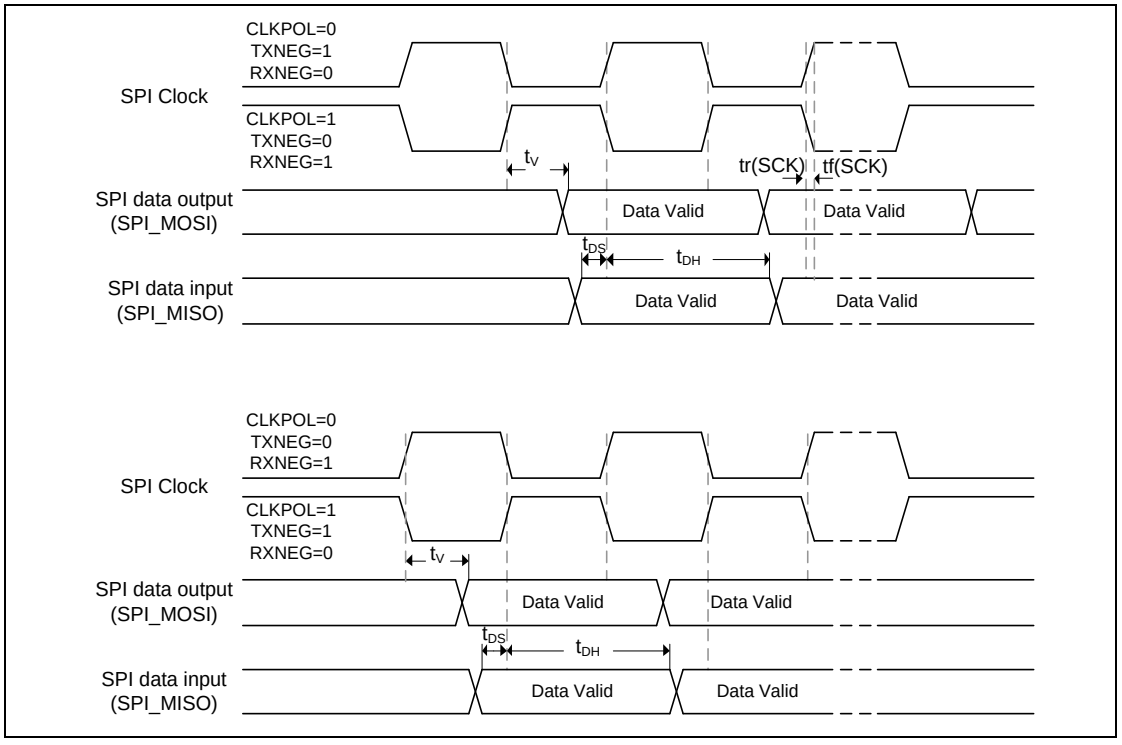


Figure 6.10-1 SPI Master Mode Timing Diagram

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI SLAVE MODE (VDD = 1.8 V~3.6V, 30 PF LOADING CAPACITOR)					
t_{SS}	Slave select setup time	3	-	-	Peripheral clock
t_{SH}	Slave select hold time	2	-	-	Peripheral clock
t_{DS}	Data input setup time	2	-	-	ns
$t_{H(SI)}$	Data input hold time	5.5	-	-	ns
$t_{a(SO)}$	Data output access time	-	-	18	ns
t_V	Data output valid time	-	18.5-	24.5	ns
$t_{H(SO)}$	Data output hold time	6	-	-	ns
SPI SLAVE MODE (VDD = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)					
t_{SS}	Slave select setup time	3	-	-	Peripheral clock
t_{SH}	Slave select hold time	2	-	-	Peripheral clock
t_{DS}	Data input setup time	2	-	-	ns
$t_{H(SI)}$	Data input hold time	6	-	-	ns
$t_{a(SO)}$	Data output access time	-	-	24	ns
t_V	Data output valid time	-	23	30	ns
$t_{H(SO)}$	Data output hold time	7	-	-	ns

Table 6.6.3-2 Dynamic Characteristics of Data Input and Output Pin in Slave Mode

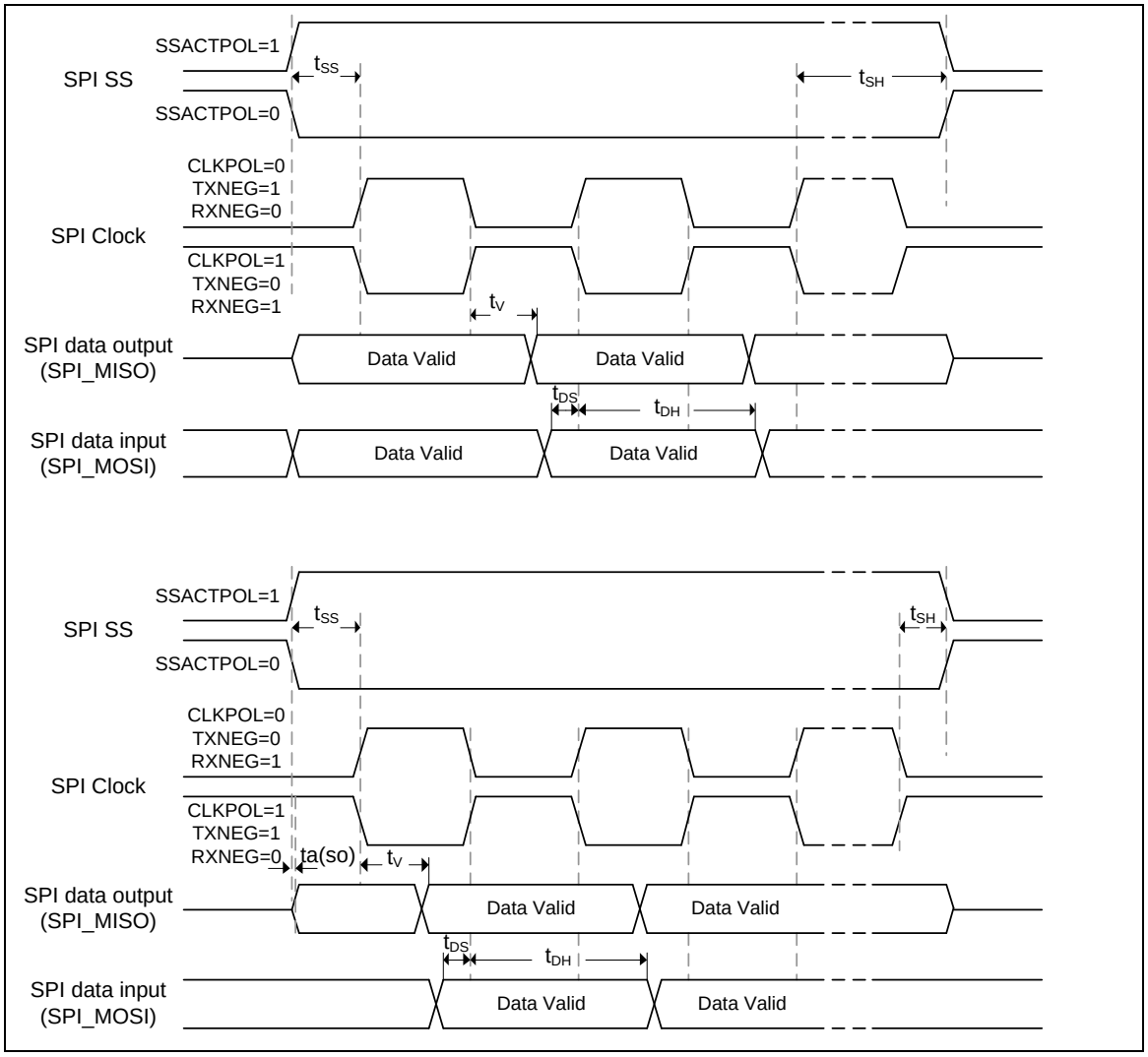


Figure 6.10-2 SPI Slave Mode Timing Diagram

6.11 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	-		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Table 6.11-1 I²S Dynamic Characteristics

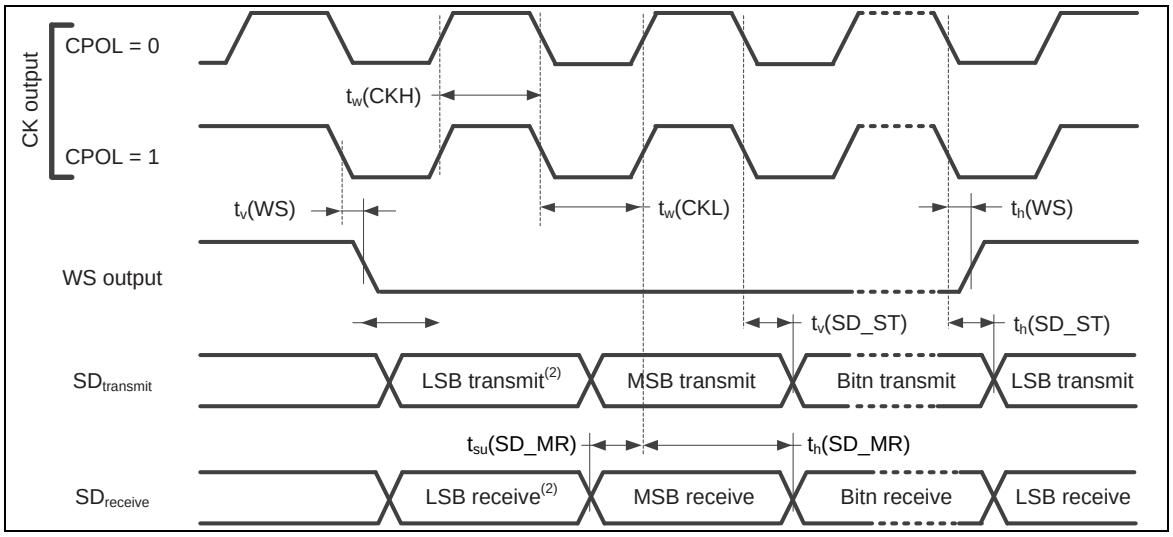


Figure 6.11-1 I²S Master Mode Timing Diagram

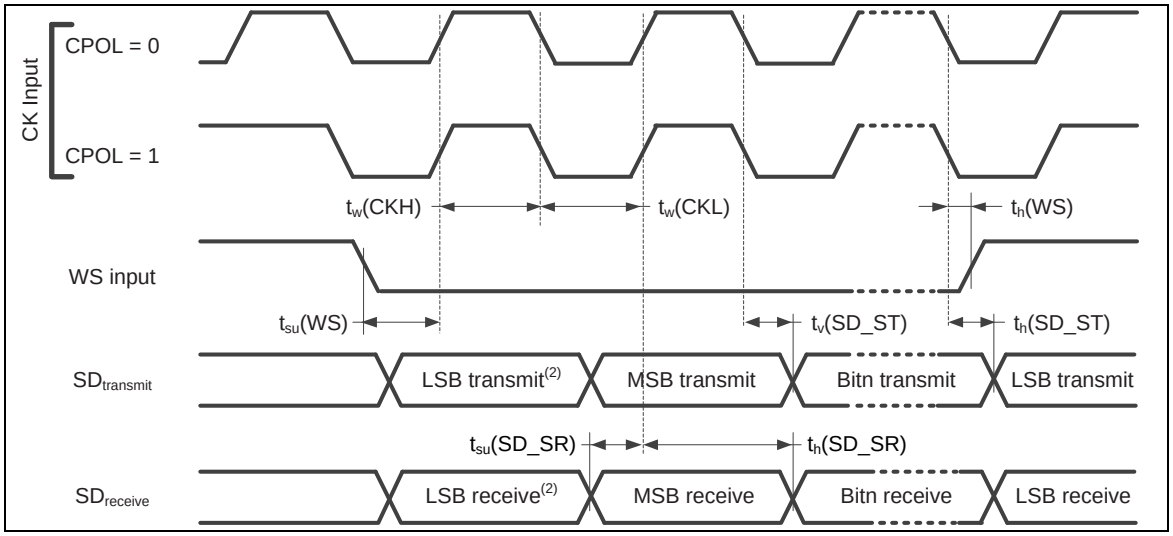


Figure 6.11-2 I²S Slave Mode Timing Diagram

7 APPLICATION CIRCUIT

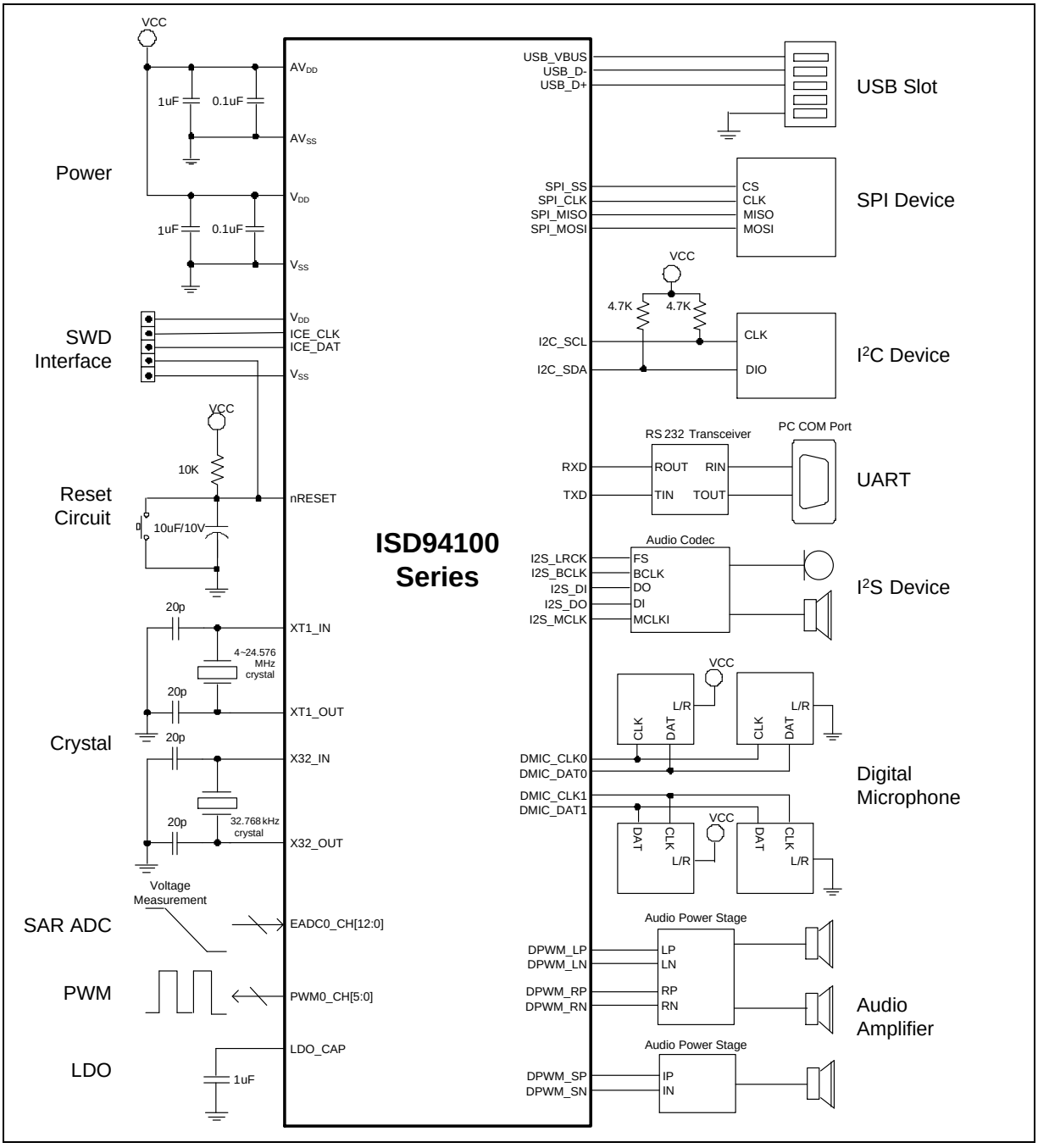
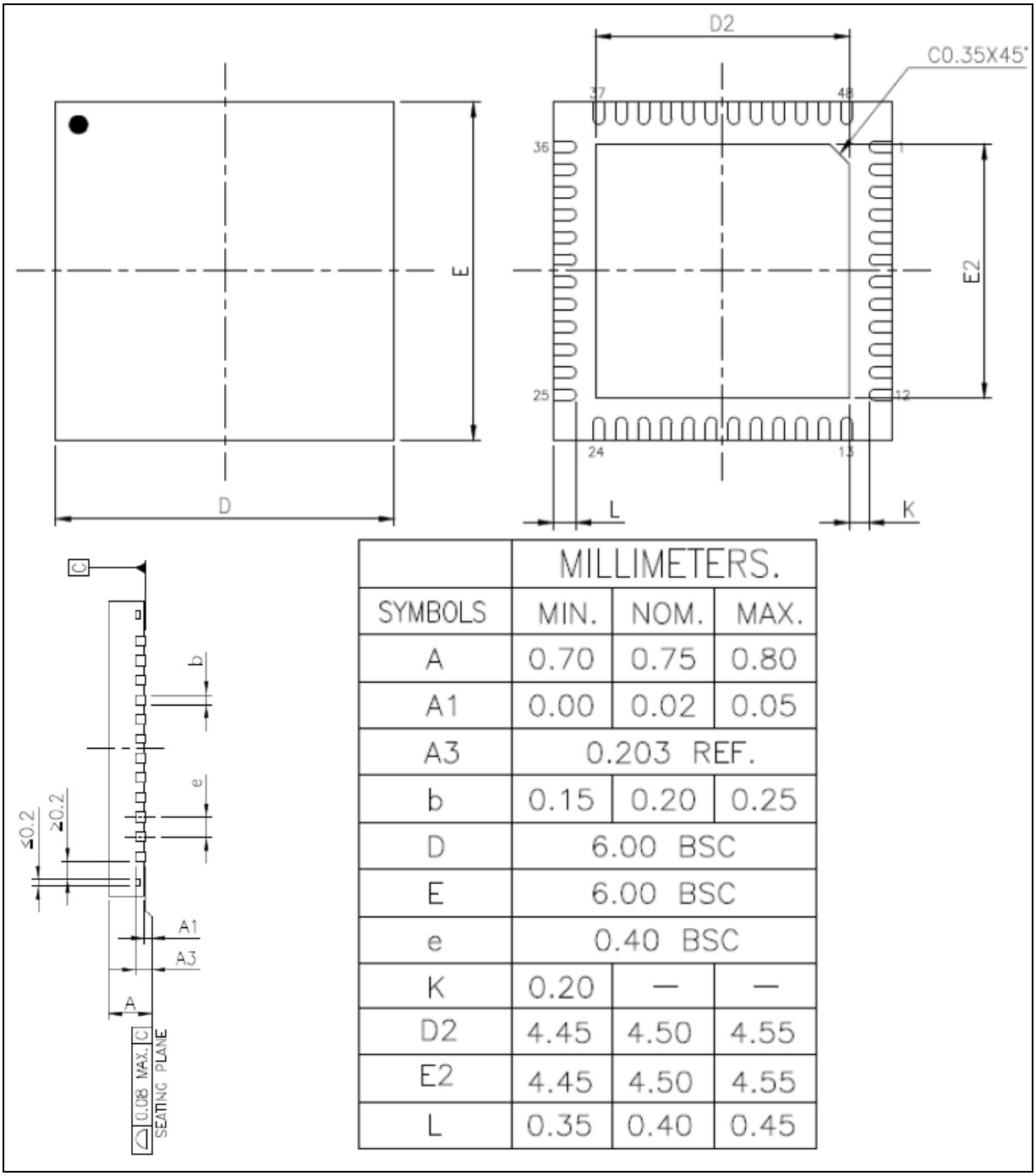


Figure 7-1 Application Circuit

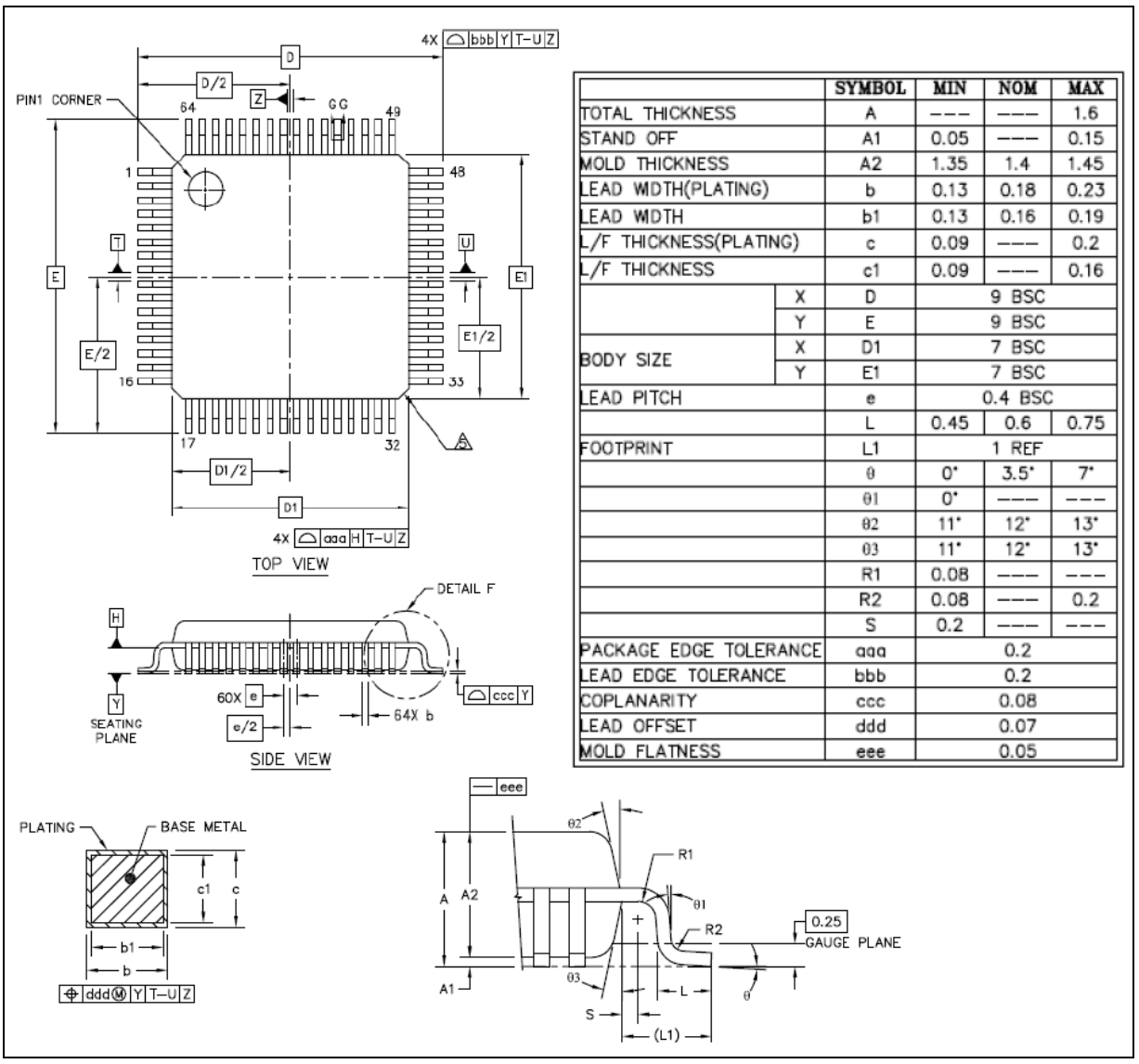
8 PACKAGE DIMENSIONS

8.1 QFN 48L (6x6x0.8 mm^3 Pitch 0.4 mm)



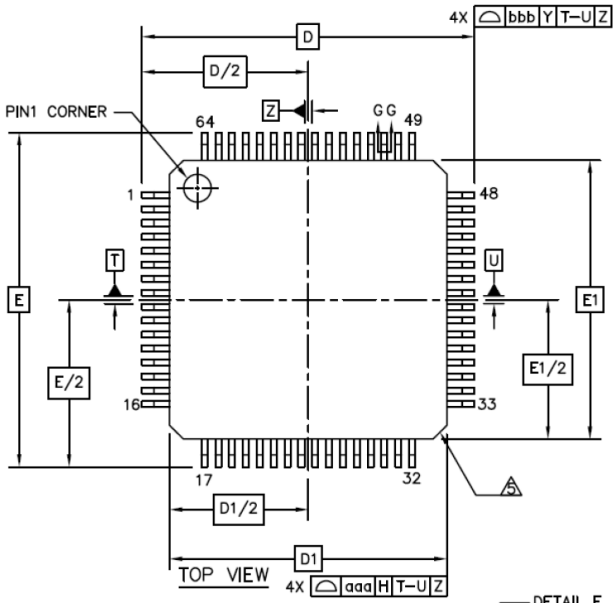
	MILLIMETERS.		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
e		0.40 BSC	
K	0.20	—	—
D2	4.45	4.50	4.55
E2	4.45	4.50	4.55
L	0.35	0.40	0.45

8.2 LQFP 64L (7x7x1.4 mm^3 footprint 2.0 mm)

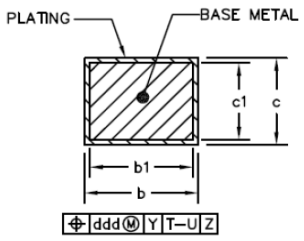


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

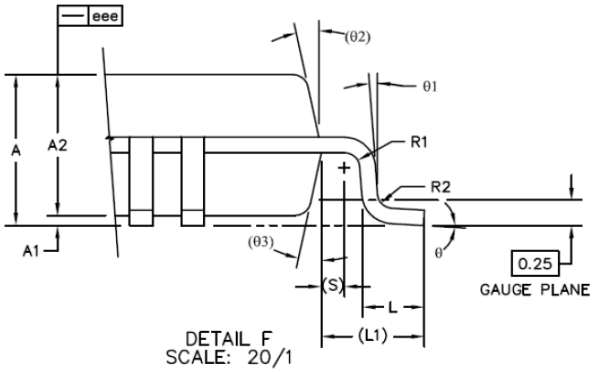
8.3 LQFP 64L (10x10x1.4 mm^3 footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	12 BSC		
	Y	E	12 BSC		
	X	D1	10 BSC		
	Y	E1	10 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	---	7°
		θ1	0°	---	---
		θ2	12° REF		
		θ3	12° REF		
		R1	0.1	---	0.2
		R2	0.1	---	0.2
		S	0.2 REF		
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		



SECTION G-G
SCALE: 100/1



DETAIL F
SCALE: 20/1

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

9 REVISION HISTORY

Date	Revision	Description
2017.10.27	1.0	1. Preliminary version release
2017.11.01	1.01	1. Figure 4.1-1 updated
2017.11.28	1.02	1. Typo correction 2. Added application circuit 3. Electrical characteristics updated. 4. Figure 6.3-1 updated.
2018.03.21	1.03	1. Maximum ADC clock frequency updated. 2. Figure 6.3-1, Figure 6.3-3, Figure 7.4-1, Section 7.4.4, Section 6.5.1, Section 6.5.2 updated 3. Minimum VDD and AVDD operation voltage updated 4. Section 8 updated
2018.03.26	1.04	1. Section 4.2.1 updated 2. Table 7.2-1, Table 7.5.2-1 updated 3. Section 7.2, Section 7.4, Section 7.5 updated
2018.05.17	1.05	1. Added part number, QFN48 package dimension and QFN48 pin diagram 2. Electrical characteristics updated 3. Parts information list and pin configuration updated
2018.06.11	1.06	1. Figure 6.3-1 updated.
2018.08.14	1.07	1. Figure 4.2-1, Table 4.1-1 and Table 4.2-1 updated.
2018.12.17	1.08	1. Added part number ISD94113ADI, Table 4.1-1 and Table 4.2-1 is updated.
2019.01.07	1.09	1. Added part number ISD94124ARI and ISD94124BRI 2. Added LQFP64 10x10 package dimensions
2019.01.29	1.10	1. Change ISD94124ARI maximum clock to 200MHz in section 4.1 Parts Information, but add note for maximum 100MHz of DMIC application.
2019.07.01	1.11	1. Added VAD Characteristics
2019.07.15	1.12	1. Application circuit is updated
2019.09.09	1.13	1. Changed cover title. 2. Changed header title.
2019.10.30	1.14	1. Removed part number I94124EDI
2019.11.06	1.15	1. Removed functional description section 2. Ordering information is updated.
2020.01.16	1.16	1. Added part no I94124CYI
2020.03.27	1.17	1. Added part no I94124SYI and I94124SDI 2. Ordering information is updated. 3. HIRC calibrated internal oscillator frequency range is updated.

2020.07.22	1.18	1. Updated Figure 4.2-1 and Table 4.2-1.
2020.08.14	1.19	1. Updated Table 4.1-1.
2020.09.23	1.20	1. Updated Figure 4.2-1
2021.03.30	1.21	1. Updated Figure 4.2-1 2. Updated Table 6.6.3-1

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